VARDHAMAN COLLEGE OF ENGINEERING

(AUTONOMOUS)

Affiliated to JNTUH, Approved by AICTE, Accredited by NAAC and ISO 9001:2008 Certified,
Shamshabad - 501 218,Hyderabad,
Telangana State, India.
www.vardhaman.org

MASTER OF TECHNOLOGY
EMBEDDED SYSTEMS
(ELECTRONICS AND COMMUNICATION ENGINEEERING)

CHOICE BASED CREDIT SYSTEM

ACADEMIC REGULATIONS, COURSE STRUCTURE AND SYLLABI FOR M.TECH. –EMBEDDED SYSTEMS UNDER AUTONOMOUS STATUS FOR THE BATCHES ADMITTED FROM THE ACADEMIC YEAR 2018 – 2019

VARDHAMAN COLLEGE OF ENGINEERING

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PRELIMINARY DEFINITIONS AND NOMENCLATURES

"Autonomous Institution / College" means an institution / college designated as autonomous institute / college by University Grants Commission (UGC), as per the UGC Autonomous College Statutes.

"Academic Autonomy" means freedom to a College in all aspects of conducting its academic programs, granted by the University for promoting excellence.

"Commission" means University Grants Commission.

"AICTE" means All India Council for Technical Education.

"University" means Jawaharlal Nehru Technological University Hyderabad.

"College" means Vardhaman College of Engineering, Hyderabad unless indicated otherwise by the context.

"Program" means:

Master of Technology (M. Tech.) Degree program

PG Degree Program: M. Tech

"Branch" means specialization in a program like M. Tech. program in Structural Engineering, M. Tech. program in Computer Science and Engineering etc.

"Course" or "Subject"means a theory or practical subject, identified by its course – number and course-title, which is normally studied in a semester. For example, B4911 English for Research Papers Writing, means a theory or practical subject, identified by its course-number and course-title, which is normally studied in a semester. The description of allocation of course code is mentioned in the table 1.

Table 1: Course Code Description

First Digit	Second Digit	Third Digit	Fourth and Fifth Digit
Indicates Program	**Indicates Regulation**	**Indicates Department**	**Indicates Course Number**
A : B. Tech. **B** : M. Tech. **C**:MBA	**1**:R11 **2**:R14 **3**:R15 **4**:R18	**1** : WMC **2** : CSE **3** : PEED **4** : DECS **5**: SE **6** : ES **7** : ED **8** : Structural Engg. **9** : Other	**01** **02** .. ..

T – Tutorial, P – Practical, D – Drawing, L - Theory, C - Credits

FOREWORD

The autonomy conferred on Vardhaman College of Engineering by UGC based on its performance as well as future commitment and competency to impart quality education. It is a mark of its ability to function independently in accordance with the norms set by the monitoring bodies like UGC and AICTE. It reflects the confidence of the UGC in the autonomous institution to uphold and maintain standards it expects to deliver on its own behalf and thus awards Degrees on behalf of the college. Thus, an autonomous institution is given the freedom to have its own **curriculum, examination system and monitoring mechanism**, independent of the affiliating University but under its observance.

Vardhaman College of Engineering is proud to win the credence of all the above bodies monitoring the quality in education and has gladly accepted the responsibility of sustaining, if not improving upon the standards and ethics for which it has been striving for more than a decade in reaching its present standing in the arena of contemporary technical education. As a follow up, statutory bodies like Academic Council and Board of Studies are constituted under the guidance of the Governing Body of the College and recommendations of the JNTUH to frame the regulations, course structure and syllabi under autonomous status.

The autonomous regulations, course structure and syllabi have been prepared after a prolonged and detailed interaction with several expertise solicited from academics, industry and research, in accordance with the vision and mission of the college in order to produce quality engineering graduates for the society.

All the faculty, parents and students are requested to go through all the rules and regulations carefully. Any clarifications, if needed, are to be sought, at appropriate time and with principal of the college, without presumptions, to avoid unwanted subsequent inconveniences and embarrassments. The cooperation of all the stake holders is sought for the successful implementation of the autonomous system in the larger interests of the college and brighter prospects of engineering graduates.

PRINCIPAL

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Institute Vision:

To be a pioneer institute and leader in engineering education to address societal needs through education and practice.

Institute Mission:

To adopt innovative student centric learning methods.

To enhance professional and entrepreneurial skills through industry institute interaction.

To train the students to meet dynamic needs of the society.

To promote research and continuing education.

Quality Policy:

We at Vardhaman College of Engineering, endeavour to uphold excellence in all spheres by adopting best practices in effort and effect.

Department Vision:

To produce competent engineers with social responsibility to address the global challenges in the field of Electronics and Communication Engineering.

Department Mission:

Promote active learning strategies to facilitate student centric learning

Provide self-learning capabilities to enhance employability and entrepreneurial skills

Inculcate human values and ethics to make learners sensitive towards societal issues

Strengthen core competencies among the learners through experiential curriculum.

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ACADEMIC REGULATIONS

M. Tech Regular Two Year Post-Graduate Programme (For the batches admitted from the Academic Year 2018–2019)

For pursuing two year PG program of study in Master of Technology (M. Tech.) offered by Vardhaman College of Engineering and herein after Vardhaman College of Engineering is referred to as VCE.

1. APPLICABILITY

All the rules specified herein, approved by the Academic Council, will be in force and applicable to students admitted from the academic year 2018-2019 onwards. Any reference to "College" in these rules and regulations stands for Vardhaman College of Engineering.

2. EXTENT

All the rules and regulations, specified herein after shall be read as a whole for the purpose of interpretation and as and when a doubt arises, the interpretation of the Chairman, Academic Council is final. As per the requirements of statutory bodies Principal, Vardhaman College of Engineering shall be the Chairman, Academic Council.

3. PROGRAMS OFFERED

Vardhaman College of Engineering, an autonomous college affiliated to JNTUH, offers the following M. Tech. programmes of study leading to the award of M. Tech. degree under the autonomous scheme.

S. No	M. Tech Courses	Offering Department	Intake
1	Computer Science and Engineering	CSE	18
2	Digital Electronics and Communication Systems	ECE	18
3	Embedded Systems	ECE	18
4	Power Electronics and Electrical Drives	EEE	18
5	Engineering Design	ME	18
6	Structural Engineering	CE	18

4. ADMISSION

Admission into first year of two Year M. Tech degree program of study:

4.1.1. Eligibility

Admission to the M. Tech degree program shall be made subject to the eligibility, qualifications and specialization prescribed by Telangana State Council of Higher Education TSCHE, Government of Telangana.

Admissions shall be made based on the rank secured in PGECET examination conducted by Telangana State Council for Higher Education (or) GATE examination for allotment of a seat by the Convener, PGECET subject to reservations prescribed by the University or policies formed by the Government of Telangana from time to time.

4.2. Admission Procedure:

Admissions are made into the first year of two year M. Tech program as per the stipulations of Telangana State Council of Higher Education (TSCHE), Government of Telangana.

(a) Category - A seats are filled by the Convener, PGECET.

(b) Category - B seats are filled by the Management.

5. MEDIUM OF INSTRUCTION

The medium of instruction and examination is English for all the courses.

6. DURATION OF THE PROGRAMS

6.1 Normal Duration

M. Tech degree program extends over a period of two academic years leading to the Degree of Master of Technology (M. Tech) of the Jawaharlal Nehru Technology University Hyderabad.

6.2 Maximum Duration

6.2.1 The maximum period within which a student must complete a full-time academic program (Course Work i.e clearing all theory subjects) is 4 years for M.Tech. If a student fails to complete the academic program within the maximum duration as specified above, he / she will be required to withdraw from the program.

6.2.2 The period is reckoned from the academic year in which the student is admitted first time into the degree programme.

7. SEMESTER STRUCTURE

The College shall follow semester pattern. An academic year shall consist of a first semester and a second semester and the summer term. Each semester shall be of 21 weeks duration and this period includes time for course work, examination preparation, and conduct of examinations. Each semester shall have a minimum of 90 working days including Examinations. The academic calendar is shown in Table 2 is declared at the start of the semester. The duration for each semester shall be a minimum of 16 weeks of instruction.

Table 2: Academic Calendar

<table>
<tr><td rowspan="4">I Year
I Semester
(21 weeks)</td><td>Instruction Period :16 weeks</td><td rowspan="2">18 weeks</td></tr>
<tr><td>Mid Semester Tests :2 weeks</td></tr>
<tr><td>Preparation & Practical Examinations</td><td>1 week</td></tr>
<tr><td>External Examinations</td><td>2 weeks</td></tr>
<tr><td colspan="2">Semester Break</td><td>2 weeks</td></tr>
<tr><td rowspan="4">I Year
II Semester
(21 weeks)</td><td>Instruction Period :16 weeks</td><td rowspan="2">18 weeks</td></tr>
<tr><td>Mid Semester Tests :2 weeks</td></tr>
<tr><td>Preparation & Practical Examinations</td><td>1 week</td></tr>
<tr><td>External Examinations</td><td>2 weeks</td></tr>
<tr><td colspan="2">Summer Vacation</td><td>4 weeks</td></tr>
<tr><td rowspan="3">II Year
I Semester
(20 Weeks)</td><td>Instruction Period and Project Phase- I</td><td rowspan="2">18 weeks</td></tr>
<tr><td>Mid semester tests</td></tr>
<tr><td>Preparation and External Examinations</td><td>2 weeks</td></tr>
<tr><td></td><td>Semester Break</td><td>2 weeks</td></tr>
<tr><td>II Year
II Semester
(18 weeks)</td><td>Project Work Phase – II</td><td>18 weeks</td></tr>
</table>

8. CHOICE BASED CREDIT SYSTEM

All the academic programs under autonomy are based on credit system. Credits are assigned based on the following norms:

8.1 The duration of each semester will normally be 21 weeks with 6 days a week. A working day shall have 6 periods each of 60 minutes duration.

1 credit per lecture period per week

2 credits for four period hours of practical

2 credits for mini project with seminar

10 credits for project work phase – I

16 credits for project work phase – II

8.2 The two year curriculum of any M. Tech Specialization of study shall have total of 68 credits. The exact requirements of credits for each course will be as recommended by the Board of Studies concerned and approved by the Academic Council.

9. COURSE REGISTRATION

9.1. A 'faculty advisor or counsellor' shall be assigned to a group of 5 students, who will advise student about the Post graduate program, its course structure and curriculum, choice/option for subjects/courses, based on their competence, progress, pre-requisites and interest.

9.2. The college Exam cell invites 'registration forms' from students before the beginning of the semester through 'on-line registration', ensuring 'date and time stamping'. The on-line registration requests for any 'current semester' shall be completed before the commencement of SEEs (Semester End Examinations) of the 'preceding semester'.

9.3. A student can apply for on-line registration, only after obtaining the 'written approval' from faculty advisor/counsellor, which should be submitted to the Examination section through the Head of the Department. A copy of it shall be retained with Head of the Department, faculty advisor/counsellor and the student.

9.4. If the student submits ambiguous choices or multiple options or erroneous entries during on-line registration for the subject(s)/course(s) under a given/specified course group/category as listed in the course structure, only the first mentioned subject/ course in that category will be taken into consideration.

9.5. Subject/course options exercised through on-line registration are final and cannot be changed or inter-changed; further, alternate choices also will not be considered. However, if the subject/course that has already been listed for registration by the Head of the Department in a semester could not be offered due to any unforeseen or unexpected reasons, then the student shall be allowed to have alternate choice either for a new subject (subject to offering of such a subject), or for another existing subject (subject to availability of seats). Such alternate arrangements will be made by the head of the department, with due notification and time-framed schedule, within the first week after the commencement of class-work for that semester.

9.6. Open electives: The students have to choose one open elective (OEC) during II year I semester from the list of open electives given. However, the student cannot opt for an open elective subject offered by their own (parent) department, if it is already listed under any category of the subjects offered by parent department in any semester.

9.7. Program Electives: The students have to choose Program elective I & II (PEC) in I year I semester, Program electives III, IV in I year II semester and Program elective V in II year I from the list of program electives given.

10. EVALUATION - DISTRIBUTION AND WEIGHTAGE OF MARKS

The performance of a student in each semester shall be evaluated subject- wise (irrespective of credits assigned) for a maximum of 100 marks. The M. Tech. project work (major project) will be evaluated for 200 marks. (100 marks for Phase – I and 100 marks for Phase – II)

10.1. For the theory subjects 70 marks shall be awarded for the performance in the Semester End Examination (SEE) and 30 marks shall be awarded for Continuous Internal Evaluation (CIE). The Final marks of Continuous Internal Evaluation is calculated based on 75% of best Marks and 25% of least marks secured in the two Mid-Term Examinations conducted. First Mid-Term examinations will be conducted in the middle of the Semester and second Mid-Term examinations during the last week of instruction. Each Mid-Term Examination shall be conducted for a total duration of 90 minutes. The question paper consist of 5

questions out of which 3 questions are to be answered, each question carrying 10 marks for a total of 30 marks. The details of the Question Paper pattern for Semester End Examination (Theory) are given below:

The Semester End Examination will be conducted for 70 marks. It consists of two parts.

i. Part A for 20 marks,

ii. Part B for 50 marks.

Part A is compulsory and consists of 5 questions, one from each unit and carrying 4 marks each. Part B consists of 5 questions carrying 10 marks each. There will be two questions from each unit and only one should be answered.

The question paper shall be set externally and valuated both internally and externally. If the difference between both the valuations is less than 15 marks, the average marks of the two valuations shall be awarded as final marks, otherwise third valuation will be conducted and the average marks of the best two valuations shall be awarded as final marks.

10.2. For practical subjects, 70 marks shall be awarded for performance in the Semester End Examinations and 30 marks shall be awarded for day-to-day performance as Internal Marks.

10.3. For conducting laboratory end examinations of all PG Programs, one internal examiner and one external examiner are to be appointed by the Principal of the College and this is to be informed to the Controller of Examinations within two weeks, before commencement of the lab end examinations. The external examiner should be selected from outside the College.

10.4. Every candidate shall be required to submit a thesis or dissertation on a topic approved by the Project Review Committee.

10.5. A Project Review Committee (PRC) shall be constituted with the Head of the Department as Chairperson, Project Supervisor and one senior faculty member of the Departments offering the M. Tech programme.

10.6. A candidate has to present in Project Work Review I, in consultation with his Project Supervisor, the title, objective and plan of action of his project work to the Project Work Review Committee (PRC) for approval within four weeks from the commencement of Second Year First Semester. Only after obtaining the approval of the PRC the student can initiate the Project work.

10.7. If a candidate wishes to change his supervisor or topic of the project, he can do so with the approval of the PRC. However, the PRC shall examine whether or not the change of topic/supervisor leads to a major change of his initial plans of project proposal. If yes, his date of registration for the project work starts from the date of change of Supervisor or topic as the case may be.

10.8. A candidate shall submit his project progress report in two stages one in II year I semester and final one at the end of II year II Semester.

10.9. The work on the project shall be initiated at the beginning of the II year I Semester and the duration of the project is two semesters. A candidate is permitted to submit Project Thesis only after successful completion of all theory and practical courses with the approval of PRC not earlier than 40 weeks from the date of approval of the project work. For the approval of PRC the candidate shall submit the draft copy of thesis to the Head of the Department and make an oral presentation before the PRC.

10.10. The Project Work Review II in II Year I Sem. carries internal marks of 100. Evaluation should be done by the PRC for 50 marks and the Supervisor will evaluate the work for the other 50 marks. The Supervisor and PRC will examine the Problem Definition, Objectives, Scope of Work, Literature Survey in the same domain and progress of the Project Work. A candidate has to secure a minimum of 50% of marks to be declared successful in Project Work Review II (Phase –I) . If he fails to obtain the minimum required marks, he has to reappear for Project Work Review-II as and when conducted.

10.11. The Project Work Review III in II Year II Sem.(Phase –II) carries 100 internal marks. Evaluation should be done by the PRC for 50 marks and the Supervisor will evaluate it for the other 50 marks. The PRC will examine the overall progress of the Project Work and decide whether or not the Project is eligible for final submission. A candidate has to secure a minimum of 50% of marks to be declared successful in Project Work Review III. If he fails to obtain the required minimum marks, he has to reappear for Project Work Review III as and when conducted. For Project Evaluation (Viva Voce) in II Year II Sem. there are external marks of 100 and it is evaluated by the external examiner. The candidate has to secure a minimum of 50% marks in Project Evaluation (Viva-Voce) examination.

10.12. After approval from the PRC, a soft copy of the thesis should be submitted for ANTIPLAGIARISM check and the plagiarism report should be submitted to the COE and to be included in the final thesis. The Thesis will be accepted for submission, if the similarity index is less than 30%. If the similarity index has more than the required percentage, the student is advised to modify accordingly and re-submit the soft copy of the thesis after one month. The maximum number of re-submissions of thesis after plagiarism check is limited to THREE. After three attempts, the admission is liable to be cancelled. The departments HODs are advised to make plagiarism check of every soft copy of theses before submissions.

10.13. Three copies of the Project Thesis certified by the supervisor shall be submitted to the department, after submission of a research paper related to the project work in any peer reviewed Journal or Scopus Indexed Conference. A copy of the submitted research paper shall be attached to thesis.

10.14. The thesis shall be adjudicated by an external examiner selected by the Principal. For this, the department HOD shall submit a panel of three examiners from among the list of experts in the relevant specialization as submitted by the supervisor concerned.

10.15. If the report of the external examiner is unsatisfactory, the candidate shall revise and resubmit the Thesis. If the report of the examiner is unsatisfactory again, the thesis shall be summarily rejected. Subsequent actions for such dissertations may be considered, only on the specific recommendations of the external examiner and /or Project work Review Committee. No further correspondence in this matter will be entertained, if there is no specific recommendation for resubmission.

10.16. If the report of the examiner is satisfactory, the Head of the Department shall coordinate and make arrangements for the conduct of Project Viva- Voce examination. The Project Viva-Voce examination shall be conducted by a board consisting of the Supervisor, Head of the Department and the external examiner who adjudicated the Thesis. The candidate has to secure a minimum of 50% of marks in Project Evaluation (Viva-Voce) examination.

10.17. If he fails to fulfill the requirements as specified above, he will reappear for the Viva-Voce examination only after three months. In the reappeared examination also, if he fails to fulfill the requirements, he will not be eligible for the award of the degree, unless he is asked to revise and resubmit his project work by the board within a specified time period . The Project Viva-Voce External examination marks must be submitted to the Exam cell on the day of the examination.

10.18. A candidate shall be given one chance for a maximum of Three Theory subjects for Improvement of Internal evaluation marks for which the candidate has to re-register for the chosen subjects and fulfill the academic requirements.

10.19. For each subject, the candidate has to pay a fee equivalent to one third of the semester tuition fee and the amount is to be remitted in the form of D.D. in favour of the Principal, Vardhaman College of Engineering payable at Hyderabad along with the requisition through the concerned Head of the Department.

10.20. Audit course examination will be conducted at the end of the semester through open book system and evaluated internally.

11. ATTENDANCE REQUIREMENTS TO APPEAR FOR THE SEMESTER-END EXAMINATION

11.1. A student shall be eligible to appear for semester-end examinations if he acquires a minimum of 75% of attendance in aggregate of all the subjects in a semester.

11.2. Condonation of shortage of attendance in aggregate up to 10% (65% and above and below 75%) in each semester may be granted by the College Academic Council.

11.3. Shortage of attendance below 65% in aggregate shall in no case be condoned.

11.4. Students whose shortage of attendance is not condoned in any semester are not eligible to take their semester-end examination of that class and their registration shall stand cancelled.

11.5. A student will not be promoted to the next semester unless he satisfies the attendance requirements of the current semester. The student may seek readmission for the semester when offered next. He will not be allowed to register for the subjects of the semester while he is in detention. A student detained due to shortage of attendance, will have to repeat that semester when offered next.

11.6. A stipulated fee shall be payable towards condonation of shortage of attendance to the College.

11.7. Attendance may also be condoned as per the recommendations of academic council for those who participate in prestigious sports, co-curricular and extra-curricular activities provided as per the Govt. of Telangana norms in vogue.

12. ACADEMIC REQUIREMENTS FOR PROMOTION / COMPLETION OF REGULAR M.TECH PROGRAMME OF STUDY

The following academic requirements have to be satisfied in addition to the attendance requirements for promotion / completion of regular M. Tech programme of study.

i. A student shall be deemed to have satisfied the minimum academic requirements for each theory, and practical, if he secures not less than **40%** of marks in the semester-end examination and a minimum of **50%** of marks in the sum of the internal evaluation and semester - end examination taken together.

ii. In case of Mini Project with seminar, a student shall be deemed to have satisfied the minimum academic requirements and earned the credits allotted to each of them if he secures not less than **50%** of marks.

iii. In case of project work, a student shall be deemed to have satisfied the minimum academic requirements and earned the credits allotted if he secures not less than **50%** of marks on the aggregate in the internal evaluation and external end-evaluation taken together.

iv. A student shall register for all the **68** credits and earn all the 6**8** credits. Grades obtained in all the 68 credits shall be considered for the award of the class based on aggregate of grades (CGPA).

v. Students who are detained for want of attendance (or) who have not fulfilled academic requirements (or) who have failed after having undergone the course in earlier regulations (or) have discontinued and wish to continue the course are eligible for admission into the unfinished semester from the date of commencement of class work with the same (or) equivalent subjects as and when subjects are offered, and pursue the remaining course work with the academic regulations of the batch into which such students are readmitted. However, all such readmitted students shall earn all the credits of subjects they have pursued for completion of the course.

13. SUPPLEMENTARY EXAMINATION

Supplementary examinations for the odd semester shall be conducted with the regular examinations of even semester and vice versa, for those who appeared and failed in regular examinations. Such of the candidates writing supplementary examinations may have to write more than one examination per day, if it is scheduled.

14. REVALUATION

Students shall be permitted to apply for revaluation (Only for theory courses) after the declaration of semester end examination results within due dates by paying prescribed fee. After revaluation if there is any betterment in the grade then improved grade will be considered. Otherwise old grade shall be retained.

15. TRANSITORY REGULATIONS

Students who are detained for want of attendance (or) who have not fulfilled academic requirements (or) who have failed after having undergone the course in earlier regulations (or) have discontinued and wish to continue the course are eligible for admission into the unfinished semester from the date of commencement of class work with the same (or) equivalent subjects as and when subjects are offered, and pursue the remaining course work with the academic regulations of the batch into which such students are readmitted. A regular student has to satisfy all the eligibility requirements within the maximum stipulated period of four years for the award of M. Tech. Degree.

16. TRANSCRIPTS

After successful completion of the entire programme of study, a transcript containing performance of all academic years will be issued as a final record. Transcripts will also be issued, if required, after payment of requisite fee. Partial transcript will also be issued up to any point of study to a student on request, after payment of requisite fee.

17. AWARD OF DEGREE

The degree will be conferred and awarded by Jawaharlal Nehru Technological University Hyderabad on the recommendations of the Chairman, Academic Council.

17.1. Eligibility

A student shall be eligible for the award of M. Tech. Degree, if he fulfils all the following conditions:

i. Registered and successfully completed all the components prescribed in the programme of study to which he is admitted.

ii. Successfully acquired the minimum required credits as specified in the curriculum corresponding to the branch of study within the stipulated time.

iii. Obtained not less than 50% of marks (minimum requirement for declaring as passed).

iv. Has no dues to the college, hostel, and library etc. and to any other amenities provided by the College.

v. No disciplinary action is pending against him.

17.2. Award of Class

After a student has satisfied the requirement prescribed for the completion of the Program and is eligible for the award of M. Tech. Degree, he shall be placed in one of the following four classes shown in Table 3:

Table 3: Declaration of Class based on CGPA (Cumulative Grade Point Average)

Class Awarded	Grades to be Secured	
First Class with Distinction	≥ 7.75 CGPA	From the aggregate marks secured from 68 Credits
First Class	=6.75 to <7.75 CGPA	
Pass Class	=6.0 to <6.75 CGPA	
Fail	Below 6.0 CGPA	

17.3. Letter Grade and Grade Point

It is necessary to provide equivalence of percentages and/or Class awarded with Grade Point Average (GPA). This shall be done by prescribing certain specific thresholds in averages for Distinction, First Class and Pass Class, as mentioned in Table 4.

Table 4: Percentage Equivalence of *Grade Points* (For a 10-Point Scale)

Grade	Grade Points (GP)	Percentage of Marks
O	10	≥ 90
A+	9	≥ 80 and <90
A	8	≥70 and < 80
B+	7	≥ 60 and <70
B	6	≥ 50 and <60
F	0	Below 50
AB	0	ABSENT

To calculate the final percentage of marks equivalent to the computed CGPA, the following formula may be used.

Percentage of marks = (CGPA-0.5) X 10

Semester Grade Point Average (SGPA)

The SGPA is the ratio of sum of the product of the number of credits with the grade points scored by a student in all the courses taken by a student and the sum of the number of credits of all the courses undergone by a student, i.e.

SGPA (S_i) = $\sum (C_i \times G_i) / \sum C_i$

Where C_i is the number of credits of the i^{th} course and G_i is the grade point scored by student in the i^{th} course.

Cumulative Grade Point Average (CGPA)

The CGPA is also calculated in the same manner taking into account all the courses undergone by a student over all the semesters of a program, i.e.

$$\mathbf{CGPA = \sum (C_i \times S_i) / \sum C_j}$$

Where $\mathbf{S_i}$ is the SGPA of the $\mathbf{i}^{th}$ semester and $\mathbf{C_i}$ is the total number of credits in that semester.

18. REGISTRATION

Each student has to compulsorily register for course work at the beginning of each semester as per the schedule mentioned in the Academic Calendar. It is absolutely compulsory for the student to register for courses in time.

19. TERMINATION FROM THE PROGRAM

The admission of a student to the program may be terminated and the student is asked to leave the college in the following circumstances:

i. The student fails to satisfy the requirements of the program within the maximum period stipulated for that program.

ii. The student fails to satisfy the norms of discipline specified by the institute from time to time.

20. CURRICULUM

21.1. For each program being offered by the Institute, a Board of Studies (BOS) is constituted in accordance with AICTE / UGC / JNTUH statutes.

21.2. The BOS for a program is completely responsible for designing the curriculum once in three years for that program.

21. WITH-HOLDING OF RESULTS

If the candidate has not paid any dues to the college / if any case of indiscipline / malpractice is pending against him, the results of the candidate will be withheld. The issue of the degree is liable to be withheld in such cases.

22. GRIEVANCES REDRESSAL COMMITTEE

"Grievance and Redressal Committee" (General) constituted by the principal shall deal with all grievances pertaining to the academic / administrative / disciplinary matters. The composition of the complaints cum redressal committee shall be:

Headed by Senior Faculty member
Heads of all departments

A senior lady staff member from each department (if available)

The committee constituted shall submit a report to the principal of the college, the penalty to be imposed. The Principal upon receipt of the report from the committee shall, after giving an opportunity of being heard to the person complained against, submit the case with the committee's recommendation to the Governing Body of the college. The Governing Body shall confirm with or without modification the penalty recommended after duly following the prescribed procedure.

23. MALPRACTICE PREVENTION COMMITTEE

A malpractice prevention committee shall be constituted to examine and punish the students who does malpractice / behaves indiscipline in examinations. The committee shall consist of:

Principal

Subject expert of which the subject belongs to

Head of the department of which the student belongs to

The invigilator concerned

In-charge Examination branch of the college

The committee constituted shall conduct the meeting on the same day of examination or latest by next working day to the incidence and punish the student as per the guidelines prescribed by the JNTUH from time to time.

Any action on the part of candidate at the examination like trying to get undue advantage in the performance at examinations or trying to help another, or derive the same through unfair means is punishable according to the provisions contained hereunder. The involvement of the Staff, who are in charge of conducting examinations, valuing examination papers and preparing / keeping records of documents relating to the examinations in such acts (inclusive of providing incorrect or misleading information) that infringe upon the course of natural justice to one and all concerned at the examination shall be viewed seriously and recommended for award of appropriate punishment after thorough enquiry.

24. AMENDMENTS TO REGULATIONS

The Academic Council of Vardhaman College of Engineering reserves the right to revise, amend, or change the regulations, scheme of examinations, and / or syllabi or any other policy relevant to the needs of the society or industrial requirements etc., without prior notice.

25. STUDENTS' FEEDBACK

It is necessary for the Colleges to obtain feedback from students on their course work and various academic activities conducted. For this purpose, suitable feedback forms shall be devised by the College and the feedback obtained from the students regularly in confidence, by administering the feedback form in print or on-line in electronic form.

The feedback received from the students shall be discussed at various levels of decision making at the College and the changes/ improvements, if any, suggested shall be given due consideration for implementation.

26. GRADUATION DAY

The College shall have its own annual *Graduation Day* for the award of Degrees to students completing the prescribed academic requirements in each case, in consultation with the University and by following the provisions in the Statute.

The College shall institute Prizes and Awards to meritorious students, for being given away annually at the *Graduation Day.* This will greatly encourage the students to strive for excellence in their academic work.

27. AWARD OF A RANK UNDER AUTONOMOUS SCHEME

27.1. One (1) Merit Rank will be declared only for those students who have been directly admitted in VCE under Autonomous Regulations and complete the entire course in VCE only within the minimum possible prescribed time limit, i.e., 2 years for M. Tech.

27.2. A student shall be eligible for a merit rank at the time of award of degree in each branch of Master of Technology, provided the student has passed all subjects prescribed for the particular degree program in first attempt only.

27.3. Award of prizes, scholarships, or any other Honours shall be based on the rank secured by a candidate, consistent with the guidelines of the Donor, wherever applicable.

28. CONDUCT AND DISCIPLINE

28.1. Each student shall conduct himself / herself in a manner befitting his / her association with VCE.

28.2. He / she is expected not to indulge in any activity, which is likely to bring disrepute to the college.

28.3. He / she should show due respect and courtesy to the teachers, administrators, officers and employees of the college and maintain cordial relationships with fellow students.

28.4. Lack of courtesy and decorum unbecoming of a student (both inside and outside the college), wilful damage or removal of Institute's property or belongings of fellow students, disturbing others in their studies, adoption of unfair means during examinations, breach of rules and regulations of the Institute, noisy and unruly behaviour and similar other undesirable activities shall constitute violation of code of conduct for the student.

28.5. Ragging in any form is strictly prohibited and is considered a serious offence. It will lead to the expulsion of the offender from the college.

28.6. Violation of code of conduct shall invite disciplinary action which may include punishment such as reprimand, disciplinary probation, debarring from the examination, withdrawal of placement services, withholding of grades / degrees, cancellation of registration, etc., and even expulsion from the college.

28.7. Principal, based on the reports of the warden of Institute hostel, can reprimand, impose fine or take any other suitable measures against an inmate who violates either the code of conduct or rules and regulations pertaining to college hostel.

28.8. A student may be denied the award of degree / certificate even though he / she have satisfactorily completed all the academic requirements if the student is found guilty of offences warranting such an action.

28.9. Attendance is not given to the student during the suspension period.

29. OTHER ISSUES

The quality and standard of engineering professionals are closely linked with the level of the technical education system. As it is now recognized that these features are essential to develop the intellectual skills and knowledge of these professionals for being able to contribute to the society through productive and satisfying careers as *innovators, decision makers and/or leaders* in the global economy of the 21st century, it becomes necessary that certain improvements are introduced at different stages of their education system. These include:

i. Selective admission of students to a programme, so that merit and aptitude for the chosen technical branch or specialization are given due consideration.

ii. Faculty recruitment and orientation, so that qualified teachers trained in good teaching methods, technical leadership and students' motivation are available.

iii. Instructional/Laboratory facilities and related physical infrastructure, so that they are adequate and are at the contemporary level.

iv. Access to good library resources and Information & Communication Technology **(ICT)** facilities, to develop the student's *mind* effectively.

These requirements make it necessary for the College to introduce improvements like:

i. Teaching-learning process on modern lines, to provide *Add-On* Courses for *audit*/credit in a number of peripheral areas useful for students' self-development.

ii. Life-long learning opportunities for faculty, students and alumni, to facilitate their dynamic interaction with the society, industries and the world of work.

iii. Generous use of ICT and other modern technologies in everyday activities.

30. GENERAL

Where the words "he", "him", "his", "himself" occur in the regulations, they include "she", "her", "herself".

Note: Failure to read and understand the regulations is not an excuse.

MALPRACTICES RULES

DISCIPLINARY ACTION FOR / IMPROPER CONDUCT IN EXAMINATIONS

	Nature of Malpractices/Improper conduct	Punishment
	If the student:	
1. (a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the student which can be used as an aid in the subject of the examination)	Expulsion from the examination hall and cancellation of the performance in that subject only.
(b)	Gives assistance or guidance or receives it from any other student orally or by any other body language methods or communicates through cell phones with any student or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the students involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2.	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the student is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the student has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that Semester/year. The Hall Ticket of the student is to be cancelled and sent to the University.
3.	Impersonates any other student in connection with the examination.	The student who has impersonated shall be expelled from examination hall. The student is also debarred and forfeits the seat. The performance of the original student, who has been impersonated, shall be cancelled in all the subjects of the examination (including practicals and project work) already appeared and shall not be allowed to appear for examinations of the remaining subjects of that semester/year. The student is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the student is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.
4.	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the student has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The student is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the student is subject to the academic regulations in connection with forfeiture of seat.
5.	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that subject.
6.	Refuses to obey the orders of the Chief Superintendent/Assistant – Superintendent / any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in charge or any person on duty in or outside the	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the student(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The students also

	examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer-in-charge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	are debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case is registered against them.
7.	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the student has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The student is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the student is subject to the academic regulations in connection with forfeiture of seat.
8.	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the student has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The student is also debarred and forfeits the seat.
9.	If student of the college, who is not a student for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	Student of the colleges expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the student has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The student is also debarred and forfeits the seat. Person(s) who do not belong to the College will be handed over to police and, a police case will be registered against them.
10.	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the student has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year.
11.	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject and all other subjects the student has appeared including practical examinations and project work of that semester/year examinations.
12.	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the University for further action to award suitable punishment.	

COURSE STRUCTURE

M. TECH – EMBEDDED SYSTEMS

REGULATIONS: VCE--R18

I SEMESTER

Code	Subject	Periods per Week		Credits	Scheme of Examination Maximum Marks		
		L	P		Internal	External	Total
B4601	Embedded Real Time operating Systems	3	0	3	30	70	100
B4602	Microcontrollers and Programmable Digital Signal Processors	3	0	3	30	70	100
PROGRAM ELECTIVE – I		3	0	3	30	70	100
PROGRAM ELECTIVE – II		3	0	3	30	70	100
B4603	Microcontrollers & Systems Laboratory	0	4	2	30	70	100
B4604	Embedded Signal Processers Laboratory	0	4	2	30	70	100
B4001	Research Methodology and IPR	2	0	2	30	70	100
	Audit Course-I	2	0	0	30*	70*	100*
TOTAL		16	08	18	210	490	700

II SEMESTER

Code	Subject	Periods per week		Credits	Scheme of Examination Maximum Marks		
		L	P		Internal	External	Total
B4605	Computer Architecture and Parallel processing	3	0	3	30	70	100
B4606	Embedded Software Design	3	0	3	30	70	100
PROGRAM ELECTIVE – III		3	0	3	30	70	100
PROGRAM ELECTIVE – IV		3	0	3	30	70	100
B4607	Python Programming Laboratory	0	4	2	30	70	100
B4608	Embedded System Design Using PSoC Laboratory	0	4	2	30	70	100
B4609	Mini –Project	0	4	2	100	0	100
	Audit Course-II	2	0	0	30*	70*	100*
TOTAL		14	12	18	280	420	700

III SEMESTER

Code	Subject	Periods per week		Credits	Scheme of Examination Maximum Marks		
		L	P		Internal	External	Total
PROGRAM ELECTIVE –V		3	0	3	30	70	100
OPEN ELECTIVE		3	0	3	30	70	100
B4610	Major Project Phase –I	0	20	10	100	0	100
TOTAL		6	20	16	160	140	300

IV SEMESTER

Code	Subject	Periods per week		Credits	Scheme of Examination Maximum Marks		
		L	P		Internal	External	Total
B4611	Major Project Phase –II	0	32	16	30	70	100
TOTAL		0	32	16	30	70	100

PROGRAM ELECTIVES			
PROGRAM ELECTIVE – I		PROGRAM ELECTIVE – II	
Code	Subject	Code	Subject
B4651	Embedded system design	B4654	Embedded Linux
B4652	Programming Languages for Embedded Software	B4655	Soft Computing
B4653	System On Chip Architecture	B4656	System Modeling and Simulation
PROGRAM ELECTIVE – III		PROGRAM ELECTIVE – IV	
Code	Subject	Code	Subject
B4657	Hardware Software Co Design	B4660	Network Security and Cryptography
B4658	IoT and its Applications	B4661	Robotics and Automation
B4659	Device Driver Development	B4662	Embedded Network and protocols
PROGRAM ELECTIVE – V			
Code	Subject		
B4663	Embedded Control Systems		
B4664	Embedded Wireless Sensor Networks		
B4665	Electronic Product Design and Reliability Engineering		
OPEN ELECTIVES		AUDIT COURSE-I & II	
B4901	Business Analytics	B4911	English for Research Papers Writing
B4902	Industrial safety	B4912	Disaster Management
B4903	Operations Research	B4913	Sanskrit for Technical Knowledge
B4904	Cost Management of Engineering Projects	B4914	Value Education
B4905	Composite Materials	B4915	Constitution of India
B4906	Waste to Energy	B4916	Pedagogy Studies
		B4917	Stress Management by Yoga
		B4918	Personality Development through Life Enlightenment skills.

SYLLABI FOR
I YEAR I SEMESTER

VARDHAMAN COLLEGE OF ENGINEERING
(AUTONOMOUS)

M. Tech. ES I SEMESTER

EMBEDDED REAL TIME OPERATING SYSTEMS

Course Code: **B4601**

L	T	P	C
3	0	0	3

SYLLABUS:

UNIT - I

BASIC REAL-TIME CONCEPTS: Terminology, Real-Time System Design Issues, Example Real-Time Systems, Common Misconceptions, Brief History; Hard Vs Soft Real-Time Systems.

A REFERENCE MODEL OF REAL TIME SYSTEMS: Processors and Resources, Temporal Parameters of real Time Work load, Periodic task model precedence constraints and data dependency, functional parameters, Resource Parameters of jobs and parameters of resources.

UNIT - II

SCHEDULING: Commonly used Approaches to Real Time Scheduling Clock Driven, Weighted Round Robin, Priority Driven, Dynamic Vs State Systems, Effective release time and Deadlines, Offline Vs Online Scheduling.

INTERTASK COMMUNICATION AND SYNCHRONIZATION: Buffering Data, Time-Relative Buffering, Ring Buffers, Mailboxes, Queues, Critical Regions, Semaphores, Other Synchronization Mechanisms, Deadlock, Priority Inversion.

UNIT - III

REAL TIME OPERATING SYSTEMS PROGRAMMING TOOLS: Operating Systems Services, I/O Subsystems, RT and Embedded Systems OS, Interrupt Routine in RTOS Environment, Micro C/OS-II- Need of a well Tested & Debugged RTOs, Use of µCOS-II.

UNIT - IV

REAL TIME COMMUNICATION: Model of Real Time communication, Priority based service disciplines for switched networks, Weighted Round Robin Service disciplines, Medium Access-Control protocols of Broadcast networks, internet and Resource Reservation Protocols, Real Time Protocol, Communication in Multicomputer Systems.

UNIT – V

VX WORKS: Memory managements task state transition diagram, pre-emptive priority, Scheduling context switches-semaphore- Binary mutex, counting watch dugs, I/O system.

CASE STUDIES: Case Studies of programming with RTOS- Case Study of Automatic Chocolate Vending m/c using µCOS RTOS, case study of sending application Layer byte Streams on a TCP/IP network, Case Study of an Embedded System for a smart card.

List of Text Books / References / Websites / Journals / Others

Text Books:

1. A. Phillip Laplante (2004), *Real Time Systems Design and Analysis,* 3rd edition, John Wiley and Sons, India.
2. Liu, Jane W. S. (2009), *Real-Time Systems*, 8th edition, Pearson Education, India.
3. Rajkamal (2008), *Embedded Systems- Architecture, Programming and Design*, 2nd edition, Tata McGraw-Hill, New Delhi, India.

Reference Books:

1. C. M. Krishna, Kang G. Shin (2010), *Real Time Systems*, Tata McGraw-Hill, New Delhi.
2. Tanenbaum (2008), *Distributed Operating Systems*, 5th edition, Pearson Education, New Delhi, India.
3. Raymond J. A. Bhur, Donald L. Bailey (1999), *An Introduction to Real Time Systems*, Prentice Hall of India, New Delhi, India.

VARDHAMAN COLLEGE OF ENGINEERING
(AUTONOMOUS)

M. Tech. ES I SEMESTER

MICROCONTROLLERS AND PROGRAMMABLE DIGITAL SIGNAL PROCESSORS

Course Code: **B4602** **LTPC 3003**

SYLLABUS:

UNIT - I

ARM Cortex-M3 processor: Applications, Programming model – Registers, Operation modes, Memory Maps, Exceptions and Interrupts, Vector Tables, Stack Memory Operations.

Memory Systems: Memory Maps, Memory Access Attributes, Bit-Band Operations, Unaligned Transfers, Exclusive Accesses.

UNIT – II

Cortex-M3 Implementation:

The Pipeline, Block Diagram, Bus Interfaces on the Cortex-M3, Other Interfaces on the Cortex-M3, The External PPB, Reset Types and Reset Signals.

UNIT - III

Exceptions: Types, Priority, Vector Tables, Interrupt Inputs and Pending behaviour, Fault Exceptions, Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller, Basic Interrupt Configuration, SYSTICK Timer, Interrupt Sequences, Exception Exits, Tail Chaining, Interrupt Latency.

LPC 17XX MICROCONTROLLER- Internal memory, GPIOs, Timers, ADC, UART and other serial interfaces, PWM, RTC, WDT.

UNIT – IV

Programmable DSP (P-DSP) Processors: Harvard architecture, Multi port memory, architectural structure of P-DSP-MAC unit, Barrel shifters, Introduction to TI DSP processor family.

VLIW architecture and TMS320C6000 series, architecture study, data paths, cross paths, Introduction to Instruction level architecture of C6000 family, Assembly Instructions memory addressing, for arithmetic, logical operations.

UNIT - V

Code Composer Studio for application development for digital signal processing, On chip peripherals, Processor benchmarking.

Recent Trends in DSP system design: FPGA based DSP system design, Design flow, Case studies.

List of Text Books / References / Websites / Journals / Others

Text Books:

1. Joseph Yiu, “The definitive guide to ARM Cortex-M3”, Elsevier, 2nd Edition.
2. Venkatramani B. and Bhaskar M. “Digital Signal Processors: Architecture, Programming and Applications” , TMH , 2nd Edition.

Reference Books:

1. Sloss Andrew N, Symes Dominic, Wright Chris, “ARM System Developer's Guide: Designing and Optimizing”, Morgan Kaufman Publication
2. Steve furber, “ARM System-on-Chip Architecture”, Pearson Education
3. Frank Vahid and Tony Givargis, “Embedded System Design”, Wiley
4. Technical references and user manuals on www.arm.com, NXP Semiconductor www.nxp.com and Texas Instruments www.ti.com

VARDHAMAN COLLEGE OF ENGINEERING
(AUTONOMOUS)

M. Tech. ES I SEMESTER

EMBEDDED SYSTEM DESIGN
(PROGRAM ELECTIVE – I)

Course Code: **B4651**

L	T	P	C
3	0	0	3

UNIT-I

INTRODUCTION: Embedded System Overview, Design Challenge, Processor Technology, IC technology, Design Technology, Trade offs

UNIT-II

CUSTOM SINGLE PURPOSE PROCESSORS: Introduction, Combinational Logic, Sequential Logic, Custom Single Purpose Processor Design, RT Level Single Purpose Processor Design, Optimizing Custom Single Purpose Processors

UNIT-III

GENERAL PURPOSE PROCESSORS: Introduction, Basic Architecture, Operation, Programmer's View, Development Environment, ASIPs, Selecting a Microprocessor, General Purpose Processor Design

STANDARD SINGLE PURPOSE PROCESSORS: Introduction, Timers Counters and Watchdog Timers, UART, Pulse Width Modulators, LCD Controllers, Keypad Controllers, Stepper Motor Controllers, Analog to Digital Convertors, Real Time Clocks

UNIT-IV

MEMORY: Introduction, Memory Write Ability and Storage Performance, Common Memory Types, Composing Memory, Memory Hierarchy and cache, Advanced RAM, Memory Management Unit.

CASE STUDY OF DIGITAL CAMERA EXAMPLE: Introduction, Introduction to a Simple Digital Camera, Requirements Specification, Design

UNIT-V

IC Technology: Introduction, Full-Custom (VLSI) IC Technology, Semi-Custom (ASIC) IC Technology, Programmable Logic Device (PLD) IC Technology

Design Technology: Introduction, Automation: Synthesis**,** Verification: Hardware/Software Co-Simulation Emulators, Reuse: Intellectual property Cores Hard, soft and firm cores, Design Process Models

List of Text Books / References / Websites / Journals / Others

Text Books:

1. Frank Vahid,Tony Givargis(2002),Embedded System Design-A Unified hardware/Software Introduction,Wiley Edition,India.

VARDHAMAN COLLEGE OF ENGINEERING
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	L	T	P	C
M. Tech. ES I SEMESTER	**3**	**0**	**0**	**3**

PROGRAMMING LANGUAGES FOR EMBEDDED SOFTWARE
(PROGRAM ELECTIVE – I)

Course Code: **B4652**

UNIT - I

Introduction to C: Characteristics of Embedded Systems , C Language Overview , Structure of a C Program , Identifiers , Name Spaces and Scope , Compilation & Linking ,MCU Boot Process , C Best Practices for Embedded Systems

Software Engineering: The Software "Life-Cycle",Why C++?,2: Designing Software: Two Approaches,Why Design?,Top-Down Design,The Object Alternative Which method is Better, TDD or OOD?,Software Reliability,Riss of Faulty Software,Testing,Applying Program Correctness Techniques

UNIT – II

Introduction to C++: Abstract Data Types, Classes and Objects,Problem: Computing with Time,DescribingDataTypesADT Implementation and Code Reuse,Information Hiding, Encapsulation, Views,Creating Encapsulated ADT's Using the C++ Class,Using Standard C++ Class Libraries,ADT's, Objects, and Object-Oriented Programming

Introduction to PERL : What Does “Perl” Stand For?,How Can I Get Perl?,How Do I Make a Perl Program? , Whirlwind Tour of Perl , Scalar Data:Numbers, Strings,Perl’s Built-in Warnings,Scalar Variables,Output with print ,the if Control Structure,Getting User Input ,the chomp Operator,The while Control Structure,The undef Value,The defined Function

UNIT - III

Lists and Arrays & Subroutines: Accessing Elements of an Array,Special Array Indices,List Literals,List Assignment,Interpolating Arrays into Strings,The foreach Control Structure,Scalar and List Context,<STDIN> in List Context

Subroutines: Defining a Subroutine ,Invoking a Subroutine,Return Values ,Arguments,Private Variables in Subroutines,Variable-Length Parameter Lists,Notes on Lexical (my) Variables,The use strict Pragma,The return Operator,Non-Scalar Return Values,Persistent, Private Variables

UNIT – IV

Input and Output : Input from Standard Input ,Input from the Diamond Operator ,The Invocation Arguments,Output to Standard Output,Formatted Output with printf,Filehandles,Opening a Filehandle,Fatal Errors with die,Using Filehandles,Reopening a Standard Filehandle,Output with say,Filehandles in a Scalar, Hashes, Regular Expressions, Matching with Regular Expressions, Processing Text with Regular Expressions

More Control Structures: The unless Control Structure,The until Control Structure,Expression Modifiers,The Naked Block Control Structure,The elsif Clause,Autoincrement and Autodecrement,The for Control Structure,Loop Controls,The Conditional Operator,Logical Operators,Exercises**.**

UNIT – V

Perl Modules, File Tests, Directory Operations: Finding Modules ,Installing Modules, Using Simple Modules,Exercises
File Tests: File Test Operators,The stat and lstat Functions,The localtime Function, Bitwise Operators, Exercises
Directory Operations: Moving Around the Directory Tree,Globbing,An Alternate Syntax for Globbing,Directory Handles,Recursive Directory Listing,Manipulating Files and Directories,Removing Files,Renaming Files,Links and

Files,Making and Removing Directories,Modifying Permissions,Changing Ownership,Changing Timestamps,Exercises

List of Text Books / References / Websites / Journals / Others

Text Books:

1. Michael J. Pont , “Embedded C”, Pearson Education, 2nd Edition, 2008
2. Randal L. Schwartz, “Learning Perl”, O’Reilly Publications, 6th Edition 2011
3. A. Michael Berman, “Data structures via C++”, Oxford University Press, 2002

Reference Books:

1. Robert Sedgewick, “Algorithms in C++”, Addison Wesley Publishing Company, 1999
2. Abraham Silberschatz, Peter B, Greg Gagne, “Operating System Concepts”, John Willey & Sons, 2005

VARDHAMAN COLLEGE OF ENGINEERING
(AUTONOMOUS)

M. Tech. ES I SEMESTER

SYSTEM ON CHIP ARCHITECTURE
(PROGRAM ELECTIVE – I)

Course Code: **B4653**

L	T	P	C
3	0	0	3

UNIT - I

INTRODUCTION TO PROCESSOR DESIGN: Abstraction in Hardware Design, MUO a Simple processor, Processor Design Trade Off, Design For Low Power Consumption.

ARM PROCESSOR AS SYSTEM–ON-CHIP: Acron RISC Machine-Architecture Inherence-Arm Programming Model-ARM Development Tools-3 and 5 Stage Pipeline ARM Organization-ARM Instruction Execution and Implementation-ARM Co-Processor Interface.

UNIT - II

ARM ASSEMBLY LANGUAGE PROGRAMMING: ARM Instruction Types, Data Transfer, Data processing and Control Flow Instructions, ARM Instruction Set, Co-Processor Instructions.

ARCHITECTURE SUPPORT FOR HIGH LEVEL LANGUAGE: Data Types, Abstraction in Software Design, Expressions, Loops, Functions and Procedures, Conditional Statements, Use of Memory.

UNIT - III

MEMORY HIERARCHY: Memory Size and Speed On-Chip, Memory-Caches, Cache Design, An example Memory Management.

ARCHITECTURAL SUPPORT FOR SYSTEM DEVELOPMENT: Advanced Microcontroller Bus Architecture (AMBA), ARM Memory Interface, ARM Reference Peripheral Specification, Hardware System Prototyping Tools, Armulator, Debug Architecture.

UNIT - IV

ARCHITECTURAL SUPPORT FOR OPERATING SYSTEMS: An Introduction to Operating Systems, ARM System Control Co Processor-CP15 Protection Unit Registers-ARM Protection Unit-CP15MMU Registers-ARM MMU Architecture-Synchronization-Context Switching Input and Output.

UNIT - V

ARM CPU CORES: The ARM710T, ARM720T and ARM730T, the ARM810, the Strong ARM SA-110.

List of Text Books / References / Websites / Journals / Others

TEXT BOOKS:

1. Steve Furber (2000), *ARM System on Chip Architecture*, 2nd edition, Addison Wesley Professional, England
2. Ricardo Reis (2004), *Design of System on a Chip: Devices and Components*, 1st edition, Springer,Netherlands.

REFERENCE BOOKS:

1. JasonAndrews(2004), *Co Verification of Hard wareand Software for ARM Systemon Chip Design Embedded Technology*, Newnes Publications,USA.
2. Prakash Rashinkar, Peter Paterson, Leena Sing L (2001), *System on Chip Verification–Methodologies and Techniques*, Kluwer Academic Publishers,USA.

VARDHAMAN COLLEGE OF ENGINEERING
(AUTONOMOUS)

M. Tech. ES I SEMESTER

EMBEDDED LINUX
(PROGRAM ELECTIVE – II)

Course Code: **B4654**

L	T	P	C
3	0	0	3

UNIT - I

BASIC CONCEPTS: What Is an Embedded System? What Does Real-Time Mean? Implications of Open Source, Real Life and Embedded Linux Systems, Design and Implementation Methodology. Types of Hosts, Generic Architecture of an Embedded Linux System, System Startup, Types of Boot Configurations, System Memory Layout.

BOOTING LINUX: Target BPR's, Linux Boot Process, The Linux Root File System, Creating the Root File System, Installing the TFTP Server, Installing Minicom, Booting the Embedded Planet, Booting the Bright star Engineering Media Engine target, Boot comparison.

UNIT - II

DEBUGGING: Introducing GDB, Local Debugging, Remote Debugging, Network Mounting the Root System.

INTERRUPTS: Linux Timing Sources, Measuring Interrupt Latency, Implementing the Race Timer.

UNIT - III

PARALLEL PORT INTERFACING: Control Using the Parallel Port, Standard Parallel Port Control with Port I/O, Standard Parallel Port Control Using PPDEV, Developing a Custom Device driver.

MEMORY INTERFACING: The Hardware Design Process, Developing Life Monitoring and Snowmaking Control for the Media-Engine.

UNIT - IV

ASYNCHRONOUS SERIAL COMMUNICATION INTERFACING: The project Trailblazer asynchronous serial hardware, Development Environment, Linux Serial Communication.

SYNCHRONOUS SERIAL COMMUNICATION INTERFACING: Temperature Sensing and Display, SPI Communication and the LM70, I2C Communication with the Philips Semiconductor.

UNIT – V

SYSTEM INTEGRATION: Integration Overview, Installing the System Integration Applications, Creating and Testing the Project Trailblazer Database, Developing the Target and CGI Integration Scripts, GUI Development, Real time Capabilities, Project Trailblazer Hardware.

List of Text Books / References / Websites / Journals / Others

TEXTBOOKS:

1. Dr. CraigHollabaugh (2004), *Embedded Linux: Hardware, Software and Interfacing*, 5th edition, Pearson Education, New Delhi, India.

2. Karim Yaghmour(2008), *Building Embedded Linux Systems*, 2nd edition, O'Reilly Media, New Delhi, India.

REFERENCE BOOKS:

1. J. Corbet, Rubini, Greg K. Hartman(2005), *Linux Device Drivers*, 3rd edition, O' Reilly Media, New Delhi, India.

2. P. Raghavan, Amol Lad, Sriram Neelakandan (2005), *Embedded Linux System Design and Development*, Auerbach Publications, CRC Press, USA.

VARDHAMAN COLLEGE OF ENGINEERING
(AUTONOMOUS)

M. Tech. ES I SEMESTER

SOFT COMPUTING
(PROGRAM ELECTIVE – II)

Course Code: **B4655**

L	T	P	C
3	0	0	3

UNIT - I

INTRODUCTION TO ARTIFICIAL NEURAL NETWORKS: Introduction, Artificial Neural Networks, Historical Development of Neural Networks, Biological Neural Networks, Comparison Between Brain and the Computer, Comparison Between Artificial and Biological Neural Networks, Network Architecture, Setting the Weights, Activation Functions, Learning Methods.

FUNDAMENTAL MODELS OF ARTIFICIAL NEURAL NETWORKS: Introduction, McCulloch – Pitts Neuron Model, Architecture, Learning Rules, Hebbian Learning Rule, Perceptron Learning Rule, Delta Learning Rule (Widrow-Hoff Rule or Least mean Square (LMS) rule, Competitive Learning Rule, Out Star Learning Rule, Boltzmann Learning, Memory Based Learning.

UNIT - II

PERCEPTRON NETWORKS: Introduction, Single Layer Perceptron Architecture- Algorithm, Application Procedure, Perception Algorithm for Several Output Classes, Perceptron Convergence Theorem, Brief Introduction to Multilayer Perceptron Networks.

FEED FORWARD NETWORKS: Back Propagation Network (BPN)- Generalized Delta Learning Rule(or) Back Propagation rule, Architecture, Training Algorithm, Selection of Parameters, Learning in Back Propagation, Application Algorithm , Local Minima and Global Minima, Merits and Demerits of Back Propagation Network, Applications, Radial Basis Function Network (RBFN), Architecture, Training Algorithm for an RBFN with Fixed Centers.

UNIT - III

ADALINE AND MADALINE NETWORKS: Introduction, Adaline-Architecture, Algorithm, Application Algorithm, Madaline- Architecture, MRI Algorithm, MRII Algorithm.

COUNTER PROPAGATION NETWORKS: Full Counter Propagation Network (Full CPN), Architecture, Training Phases of Full CPN, Training Algorithm, Application Procedure, Forward only Counter Propagation Network, Architecture, Training Algorithm, Application Procedure.

UNIT - IV

SELF ORGANIZING FEATURE MAP: Introduction, methods for Determining the Winner**,** Kohonen Self organizing Feature Maps (SOM).

ASSOCIATIVE MEMORY NETWORKS-I: Introduction, Algorithms for Pattern Association-Hebb Rule for Pattern Association, Delta Rule for Pattern Association, Extended Delta Rule,Hetero Associative Memory Neural Networks-Architecture, Application Algorithm.

UNIT - V

ASSOCIATIVE MEMORY NETWORKS-II: Auto Associative Memory Network-Architecture, Training Algorithm, Iterative Auto Associative Net,Bi-directional Associative Memory-Architecture, Types of Bi-directional Associative Memory, Application Algorithm, Hamming Distance.

APPLICATIONS OF NEURAL NETWORKS: Applications of Neural Networks in Bioinformatics, Neural Network in Health Care, Application in Pattern Recognition, Image Processing.

List of Text Books / References / Websites / Journals / Others

TEXTBOOKS:

1. S. N. Shivanandam, S. Sumati, S. N. Deepa(), *Introduction to Neural Networks Using MATLAB 6.0,* Tata McGraw-Hill, New Delhi, India.

REFERENCE BOOKS:

1. J. M. Zurada(2006), *Introduction to Artificial Neural Systems*, 3rd edition Jaico Publishers New Delhi,India.

2. Kishan Mehrotra, Chelkuri K. Mohan, Sanjay Ranka(1996), *Elements of Artificial Neural Networks*, Penram International, New Delhi,India.

3. Simon Haykin(1998) *,Artificial Neural Network* , 2nd edition Prentice Hall of India, New Delhi,India.

4. B. Yegnanarayana(2004), *Artificial Neural Networks*, Prentice Hall of India, New Delhi,India.

VARDHAMAN COLLEGE OF ENGINEERING
(AUTONOMOUS)

M. Tech. ES I SEMESTER

SYSTEM MODELING AND SIMULATION
(PROGRAM ELECTIVE – II)

Course Code: **B4656**

L	T	P	C
3	0	0	3

UNIT - I

BASIC SIMULATION MODELING: The Nature of Simulation, Systems, Models and Simulation, Discrete-Event Simulation, Time-Advance Mechanisms, Components and Organization of a Discrete-Event Simulation Model, Simulation of a Single-Server Queueing System ,Problem Statement, Intuitive Explanation, Simulation of an Inventory, Alternative Approaches to Modeling and Coding Simulations ,Steps in a Sound Simulation Study, Other Types of Simulation, Advantages, Disadvantages, and Pitfalls of Simulation.

UNIT - II

SIMULATION SOFTWARE: Introduction, Comparison of Simulation Packages with Programming Languages, Classification of Simulation Software, Desirable Software Features, General-Purpose Simulation Packages, Object-Oriented Simulation, Examples of Application-Oriented Simulation Packages.

BUILDING SIMULATION MODELS: Guidelines for determining levels of model detail, Techniques for increasing model validity and credibility.

UNIT - III

MODELING TIME DRIVEN SYSTEMS: Modeling input signals, delays, System Integration, Linear Systems, Motion Control models, numerical experimentation.

EXOGENEOUS SIGNALS AND EVENTS: Disturbance signals, state machines, Petri nets and analysis, System encapsulation.

UNIT - IV

MARKOV PROCESS: Probabilistic systems, Discrete Time Markov processes, Random walks, Poisson processes, the exponential distribution, simulating a poison process, Continuous - Time Markov processes.

EVENT DRIVEN MODELS: Simulation diagrams, Queing theory, simulating queing systems, Types of Queues, Multiple servers.

UNIT - V

SYSTEM OPTIMIZATION: System identification, Searches, Alpha/beta trackers, multidimensional optimization, modeling and simulation methodology.

List of Text Books / References / Websites / Journals / Others

TEXT BOOKS:

1. Frank L. Severance (2009), *System Modeling and Simulation - An introduction*, John Wiley & Sons, New Delhi,India.

2. Averill M. Law, W. David Kelton (2006), *Simulation Modeling and Analysis*, 3rd edition, Tata McGraw-Hill, New Delhi, India.

REFERENCE BOOKS:

1. Gordan Gephery (2005), Systems *Simulation*, Prentice Hall of India, New Delhi, India.

VARDHAMAN COLLEGE OF ENGINEERING
(AUTONOMOUS)

M. Tech. ES I SEMESTER

MICROCONTROLLERS AND SYSTEMS LAB

Course Code: **B4603**

L	T	P	C
0	0	3	2

LIST OF EXPERIMENTS:

1. Programming using Arithmetic, logical and bit manipulations instructions of 8051.
2. Develop and execute the program to interface Keyboard to the 8051 Microcontroller.
3. Develop and execute the program to interface DAC to the 8051 Microcontroller.
4. Establish Serial communication between the 8051 Microcontroller and PC.
5. Interface 8279 (Key Board and Display Controller) with 8051 Microcontroller.
6. Program to verify Timer/Counter in 8051 Microcontroller.
7. Interrupt programming in 8051 Microcontroller.
8. To develop and execute the program for UART operation in 8051.
9. Program to verify counter in 8051.
10. Develop and execute the program for synchronous transmitter.
11. Communication between two PC's using ARM processor.
12. Verify Asynchronous multiplier using ARM processor.
13. Verify Asynchronous division using ARM processor.
14. Program to understand serial communication among PC/8051/PC.

Note: All these experiments are expected to run based on ARM processor

VARDHAMAN COLLEGE OF ENGINEERING
(AUTONOMOUS)

M. Tech. ES I SEMESTER

EMBEDDED SIGNAL PROCESSORS LABORATORY

Course Code: **B4604**

L	T	P	C
0	0	3	2

LIST OF EXPERIMENTS:

Part A

Experiments to be carried out on Cortex-M3 development boards and using GNU tool chain

1. Blink an LED with software delay, delay generated using the SysTick timer.
2. System clock real time alteration using the PLL modules.
3. Control intensity of an LED using PWM implemented in software and hardware.
4. Control an LED using switch by polling method, by interrupt method and flash the LED once Every five switch presses.
5. UART Echo Test.
6. Take analog readings on rotation of rotary potentiometer connected to an ADC channel.
7. Temperature indication on an RGB LED.
8. Mimic light intensity sensed by the light sensor by varying the blinking rate of an LED.
9. Evaluate the various sleep modes by putting core in sleep and deep sleep modes.
10. System reset using watchdog timer in case something goes wrong.
11. Sample sound using a microphone and display sound levels on LEDs.

1. To develop an assembly code and C code to compute Euclidian distance between any two points
2. To develop assembly code and study the impact of parallel, serial and mixed execution
3. To develop assembly and C code for implementation of convolution operation
4. To design and implement filters in C to enhance the features of given input sequence/signal

VARDHAMAN COLLEGE OF ENGINEERING
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	L	T	P	C
M. Tech. ES I SEMESTER	**2**	**0**	**0**	**2**

RESEARCH METHODOLOGY AND IPR

Course Code: **B4001**

SYLLABUS

UNIT – I

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

UNIT – II

Effective literature studies approaches, analysis Plagiarism, and Research ethics.

UNIT – III

Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee.

UNIT – IV

Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, and development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

UNIT – V

Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications. New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc., Traditional knowledge Case Studies, IPR and IITs.

TEXT BOOKS:

1.Stuart Melville and Wayne Goddard, “Research methodology: an introduction for science& engineering students.

2.Wayne Goddard and Stuart Melville, “Research Methodology: An Introduction. REFERENCE BOOKS:

1.T. Ramappa, “Intellectual Property Rights Under WTO”, S. Chand, 2008. 2.Ranjit Kumar, 2nd Edition , “Research Methodology: A Step by Step Guide for beginners.

SYLLABI FOR
I YEAR II SEMESTER

VARDHAMAN COLLEGE OF ENGINEERING

(AUTONOMOUS)

M. Tech. ES II SEMESTER

COMPUTER ARCHITECTURE AND PARALLEL PROCESSING

Course Code: **B4605**

L	T	P	C
3	0	0	3

UNIT - I

INTRODUCTION TO PARALLEL PROCESSING: Evolution of Computer Systems, Parallelism in Uniprocessor Systems, Parallel Computer Structures, Architectural Classification Schemes, Parallel Processing Applications.

MEMORY AND INPUT-OUTPUT SUBSYSTEMS: Hierarchical Memory Structure, Virtual Memory System, Memory Allocation and Management, Cache Memories and Management, Input-output Subsystems.

UNIT - II

PRINCIPLES OF PIPELINING: Pipelining, An Overlapped Parallelism-Principles of Linear Pipelining, Classification of Pipeline Processors, General Pipelines and Reservation Tables, Instruction and Arithmetic Pipelines-Design of pipelined Instruction Units, Arithmetic Pipelines Design Examples, Multifunction and Array Pipelines.

VECTOR PROCESSING: Principles of Designing Pipelined Processors-Instruction Prefetch and Branch handling, Data Buffering and Busing Structures, Internal Forwarding and register Tagging, Hazard Detection and Resolution, Job Sequencing and Collision Prevention, Dynamic Pipelines and Reconfigurability, Vector Processing Requirements-Characteristics of Vector Processing, Multiple Vector Task Dispatching, Pipelined Vector Processing Methods.

UNIT - III

PIPELINE COMPUTERS: The Space of pipelined Computers-Vector Supercomputers, Scientific Attached Processors, Early vector Processors-Architectures of Star-100 and TI-ASC,Vector Processing in Streaming Mode, Scientific Attached Processors-Architecture of AP-120B,Back-end vector computations,FPS-164,IBM 3828 and Datawest MATP.

VECTORIZATION METHODS: Recent Vector Processors-Architecture of Cray-1,Pipeline Chaining and Vector loops, Architecture of Cyber-205,Vector processing in Cyber-205 and CDC-NASF, Fujitsu VP-200 and Special features, Vectorization and Optimization Methods-Language features in Vector Processing, Design of vectorizing Compilers, Optimization of Vector Operations, Performance Evaluation of Pipelined Operations Computers.

UNIT - IV

MULTIPROCESSOR ARCHITECTURE: Functional Structures-Loosely coupled Multiprocessors, Tightly Coupled Multiprocessors, Processor Characteristics for Multiprocessing, Interconnection Networks-Time Shared or Common Buses, Crossbar Switch and Multiport Memories, Multistage Networks for Multiprocessors, Performance of Interconnection Networks.

UNIT - V

MULTIPROCESSOR PROGRAMMING: Parallel Memory Organizations-Interleaved Memory Configurations, Performance Tradeoffs in Memory Organizations,Multicache Problems and Solutions, Multiprocessor Operating Systems-Classification of Multiprocessor Operating Systems, Software requirements for Multiprocessors, Operating System Requirements, Exploiting Concurrency for Multiprocessing-Language Features to Exploit parallelism, Detection of parallelism in Programs, Program and Algorithm Restructing.

List of Text Books / References / Websites / Journals / Others

TEXT BOOKS:

1. Kai Hwang, Faye A. Briggs (1984), *Computer Architecture and Parallel Processing*, Tata McGraw-Hill International Edition, New Delhi,India.

REFERENCE BOOKS:

2. Kai Hwang (2003), *Advanced Computer Architecture,* Tata McGraw-Hill, New Delhi,India.

VARDHAMAN COLLEGE OF ENGINEERING
(AUTONOMOUS)

M. Tech. ES II SEMESTER

EMBEDDED SOFTWARE DESIGN

Course Code: **B4606**

L	T	P	C
3	0	0	3

UNIT - I

PENTIUM PROCESSOR: Introduction to the Pentium microprocessor, special Pentium registers, Pentium, memory management.

EMBEDDED DESIGN LIFE CYCLE: Introduction, Product Specification, Hardware/software partitioning, Iteration and Implementation, Detailed hardware and software design, Hardware/Software integration, Product Testing and Release, Maintaining and upgrading existing products.

UNIT - II

SELECTION PROCESS: Packaging the Silicon, Adequate Performance, RTOS Availability, Tool chain Availability, Other issues in the Selection process, Partitioning Decision: Hardware/Software Duality, Hardware Trends, ASICs and Revision Costs.

DEVELOPMENT ENVIRONMENT: The Execution Environment, Memory Organization, System Startup. Special Software Techniques: Manipulating the Hardware, Interrupts and Interrupt service Routines (ISRs), Watchdog Times, Flash Memory, Design Methodology.

UNIT – III

BASIC TOOL SET: Host - Based Debugging, Remote Debuggers and Debug Kernels, ROM Emulator, Logic Analyzer.
BDM: Background Debug Mode, Joint Test Action Group (JTAG) and Nexus. ICE – Integrated Solution: Bullet Proof Run Control, Real time trac, Hardware Break points, Overlay memory, Timing Constrains, Usage Issue, Setting the Trigger.
Testing: Why Test? When to Test? Which Test? When to Stop? Choosing Test cases, Testing Embedded Software, Performance Testing Maintenance and Testing, The Future.

UNIT - IV

WRITING SOFTWARE FOR EMBEDDED SYSTEMS: The compilation Process, Native Versus Cross-Compilers, Runtime Libraries, Writing a Library, Using alternative Libraries, using a standard Library, Porting Kernels, C extensions for Embedded Systems, Downloading. Emulation and debugging techniques.

UNIT - V

BUFFERING AND OTHER DATA STRUCTURES: What is a buffer? Linear Buffers, Directional Buffers, Double Buffering, Buffer Exchange, Linked Lists, FIFOs, Circular Buffers, Buffer Under run and Overrun, Allocating Buffer Memory, Memory Leakage. Memory and Performance Trade-offs.

List of Text Books / References / Websites / Journals / Others

TEXT BOOKS:

1. Arnold S Burger (2002), *Embedded Systems Design: Introduction to Processes, Tools, Techniques*, CMP Books,USA.

2. Steave Heath (2003), *Embedded Systems Design*, 2nd edition, Newnes Publications,Burlington.

REFERENCE BOOKS:

1. Andrew N. Sloss, Dominic Symes, Cheris Wright(), ARM *Systems Developers Guide Designing and Optimizing System Software*, Elsevier Publication,San Fransisco.
2. Daniel P. Bovet, Marco Cesati (2005), *Understanding the Linux Kernel*, 3rd edition, O'Reilly Media,USA.

VARDHAMAN COLLEGE OF ENGINEERING
(AUTONOMOUS)

M. Tech. ES II SEMESTER

HARDWARE SOFTWARE CODESIGN
(PROGRAM ELECTIVE – III)

Course Code: **B4657**

L	T	P	C
3	0	0	3

UNIT - I

CO DESIGN ISSUES: Co- design models, architectures, languages, and a generic co-design methodology.

CO SYNTHESIS ALGORITHMS: Hardware software synthesis algorithms, hardware – software partitioning distributed system co-synthesis.

UNIT - II

PROTOTYPING AND EMULATION: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure.

TARGET ARCHITECTURES: Architecture specialization techniques, system communication infrastructure, target architecture and application system classes, architecture for control dominated systems (8051-architectures for high performance control), architecture for data dominated systems (ADSP21070, TMS320C70), mixed systems.

UNIT - III

COMPILATION TECHNIQUES AND TOOLS FOR EMBEDDED PROCESSOR ARCHITECTURES: Modern embedded architectures, embedded software development needs, compilation technologies practical consideration in a compiler development environment.

DESIGN SPECIFICATION AND VERIFICATION: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification.

UNIT – IV

LANGUAGES FOR SYSTEM LEVEL SPECIFICATION AND DESIGN-I: System – level specification, design representation for system level synthesis, system level specification languages.

UNIT - V

LANGUAGES FOR SYSTEM LEVEL SPECIFICATION AND DESIGN-II: Heterogeneous specifications and multi language co-simulation the Cosyma system and Lycos system.

List of Text Books / References / Websites / Journals / Others

TEXT BOOKS:

1. Jorgen Staunstrup, Wayne Hendrix Wolf (2002), *Hardware / software co- design Principles and Practice*, kluwer academic publishers, USA.

REFERENCE BOOKS:

1. Patrick R. Schaumont (2010), *A Practical Introduction to Hardware/Software Do-design*, Springer,USA.
2. Giovanni De Micheli, Mariagiovanna Sami (1996), *Hardware/Software Co-design*, Kluwer Academic,USA.

VARDHAMAN COLLEGE OF ENGINEERING
(AUTONOMOUS)

M. Tech. ES II SEMESTER

IOT AND APPLICATIONS
(PROGRAM ELECTIVE – III)

Course Code: **B4658**

L	T	P	C
3	0	0	3

UNIT-I:

INTRODUCTION TO INTERNET OF THINGS: Introduction, Definition & Characteristics of IoT ,Physical Design of IoT , Logical Design of IoT, IoT Enabling Technologies, IoT Levels & Deployment Templates

DOMAIN SPECIFIC IOTS: Introduction, Home Automation, Cities, Environment, Energy, Retail, Logistics, Agriculture, Industry, Health & Lifestyle

UNIT-II

IoT , M2M and IoT SYSTEM MANAGEMENT WITH NETCONF-YANG: Introduction, M2M, Difference between IoT and M2M, SDN and NFV for IoT

IoT SYSTEM MANAGEMENT WITH NETCONF-YANG: Need for IoT Systems Management, Simple Network Management Protocol (SNMP), Network Operator Requirements, NETCONF, YANG, IoT Systems Management with NETCONF-YANG

UNIT-III

IoT PLATFORMS DESIGN METHODOLOGY: Introduction, IoT Design Methodology, Case Study on IoT System for Weather Monitoring, Motivation for Using Python

IoT SYSTEMS - LOGICAL DESIGN USING PYTHON : Introduction ,Installing Python ,Python Data Types & Data Structures, Control Flow ,Functions , Modules , Packages , File Handling , Date/Time Operations , Classes ,Python Packages of Interest for IoT

UNIT-IV

IoT PHYSICAL DEVICES & ENDPOINTS: What is an IoT Device, Exemplary Device: Raspberry Pi, About the Board, Linux on Raspberry Pi, Raspberry Pi Interface, Programming Raspberry Pi with Python, Other IoT Devices

IoT PHYSICAL SERVERS & CLOUD OFFERINGS: Introduction to Cloud Storage Models & Communication APIs, WAMP - AutoBahn for IoT, Xively Cloud for IoT, Python Web Application Framework ,Designing a RESTful Web API, Amazon Web Services for IoT, SkyNet IoT Messaging Platform

UNIT V

CASE STUDIES ILLUSTRATING IOT DESIGN: Introduction, Home Automation Cities, Environment, Agriculture, Productivity Applications

List of Text Books / References / Websites / Journals / Others

TEXT BOOKS:

1. Arshdeep Bahga,Vijay Madisetti(2015),"Internet of Things A Hands-On Approach",University Press,India.

VARDHAMAN COLLEGE OF ENGINEERING
(AUTONOMOUS)

M. Tech. ES II SEMESTER

DEVICE DRIVER DEVELOPMENT
(PROGRAM ELECTIVE – III)

Course Code: **B4659**

L	T	P	C
3	0	0	3

UNIT - I

INTRODUCTION: The Role of the Device Driver, Splitting the Kernel, Classes of Devices and Modules, Security Issues, Kernel Modules Versus Applications, Compiling and Loading, The Kernel Symbol Table, Preliminaries, Initialization and Shutdown, Module Parameters.

CHAR DRIVERS AND DEBUGGING TECHNIQUES: The Design of scull, Major and Minor Numbers, Some Important Data Structures, Char Device Registration, open and release, scull's Memory Usage, read and write, Playing with the New Devices, Debugging Support in the Kernel, Debugging by Printing, Debugging by Querying, Debugging by Watching, Debugging System Faults, Debuggers and Related Tools.

UNIT - II

CONCURRENCY AND RACE CONDITIONS: Pitfalls in scull, Concurrency and Its Management, Semaphores and Mutexes, Completions, Spinlocks Locking Traps, Alternatives to Locking.

ADVANCED CHAR DRIVER OPERATIONS: IOCTL, Blocking I/O, poll and select, Asynchronous Notification, Seeking a Device, Access Control on a Device File, Measuring Time Lapses, Knowing the Current Time, Delaying Execution, Kernel Timers, Task lets.

UNIT - III

MEMORY ALLOCATION: The Real Story of Kmalloc, Look aside Caches, get_free_page and Friends, Vmalloc and Friends, Per-CPU Variables, Obtaining Large Buffers.

COMMUNICATING WITH HARDWARE: I/O Ports and I/O Memory, Using I/O Ports, An I/O Port Example, Using I/O Memory.

UNIT - IV

INTERRUPT HANDLING: Preparing the Parallel Port, Installing an Interrupt Handler, Implementing a Handler, Top and Bottom Halves, Interrupt Sharing, Interrupt-Driven I/O.

UNIT - V

DATA TYPES IN THE KERNEL: Use of Standard C Types, Assigning an Explicit Size to Data Items, Interface-Specific Types, Other Portability Issues, Linked Lists, A Simple case study.

List of Text Books / References / Websites / Journals / Others

TEXT BOOKS:

1. Jonathan Corbet, Alessandro Rubini, Greg Kroah-Hartman(2009), *Linux Device Drivers*, 3rd edition, O'Reilly, Publishers,California.

2. Sreekrishnan Venkateswaran(2008), *Essential Linux Device Drivers*, Prentice Hall Publishers,Boston.

REFERENCE BOOKS:

1. Robert Love (2010), *Linux Kernel Development*, 3rd edition, Addison Wesley,USA.

2. Christopher Hallinan(2010), *Embedded Linux Primer: A Practical Real-World Approach*, 2nd edition, Prentice Hall Publishers, Boston.

VARDHAMAN COLLEGE OF ENGINEERING
(AUTONOMOUS)

M. Tech. ES II SEMESTER

NETWORK SECURITY AND CRYPTOGRAPHY
(PROGRAM ELECTIVE – IV)

Course Code: **B4660**

L	T	P	C
3	0	0	3

UNIT - I

INTRODUCTION SECURITY ATTACKS: Interruption, interception, modification and fabrication.

SECURITY SERVICES: Confidentiality, authentication, integrity, non repudiation, access control and availability.
SECURITY MECHANISMS: A model for internetwork security, internet standards and RFCs, conventional encryption principles, ceaser cipher, hill cipher, poly and mono alphabetic cipher.

UNIT - II

ENCRYPTION PRINCIPLES: Conventional encryption algorithms: Feistal structure, DES algorithm, S: Boxes, Triple DES, advanced data encryption standard (AES), cipher block modes of operation, location of encryption devices, Key distribution Approaches.

CRYPTOGRAPHY AND APPLICATIONS : Public key cryptography principles, public key cryptography algorithms, digital signatures, RSA, elliptic algorithms, digital certificates, certificate authority and key management, Kerberos, X.509, directory authentication service. Message authentication, secure hash functions and HMAC.

UNIT - III

ELECTRONIC MAIL SECURITY: Email privacy, PGP operations, radix: 64 conversions, key management for PGP, PGP trust model, multipurpose internet mail extension (MIME), secure/MIME(S/MIME).

IP SECURITY ARCHITECTURE AND SERVICES: IP security overview, IP security architecture, security association, authentication header, encapsulating security payload, combining security associations and key management, OAKELY key determination protocol, ISAKMP.

UNIT - IV

WEB SECURITY: Web security considerations, secure socket layer (SSL) and transport layer security (TLS), secure electronic transaction (SET).

NETWORK MANAGEMENT SECURITY: Basic concepts of SNMP, SNMPv1 community facility and SNMPv3. System Security, intruders, intrusion techniques, intrusion detection, password management, bot nets.

UNIT - V

MALICIOUS SOFTWARE: Viruses and related threats, virus counter measures, distributed denial of service attacks.
FIREWALLS: Firewall design principles, trusted systems, common criteria for information technology security evolution.

List of Text Books / References / Websites / Journals / Others

TEXT BOOKS:

1. William Stallings (2007), *Network Security Essentials (Applications and Standards*), 3rd Edition, Pearson Education, New Delhi, India.
2. William Stallings (1998), *Cryptography and network Security*, 3rd Edition, Prentice Hall of India, New Delhi, India.

REFERENCE BOOKS:

1. Eric Maiwald (2004), *Fundamentals of Network Security*, Dreamtech press, India.
2. Charlie Kaufman, Radia Perlman, Mike Speciner (2002), *Network Security: Private Communication in a Public World*, 2nd Edition, Pearson Education, India.
3. Robert Bragg, Mark Rhodes (2004), *Network Security: The Complete Reference*, Tata Mcgraw Hill, New Delhi.
4. Buchmann (2004), *Introduction to Cryptography*, 2nd Edition, Springer, USA.

VARDHAMAN COLLEGE OF ENGINEERING
(AUTONOMOUS)

M. Tech. ES II SEMESTER

ROBOTICS AND AUTOMATION
(Professional Elective - IV)

Course Code: **B4661**

L	T	P	C
3	0	0	3

UNIT - I

INTRODUCTION TO ROBOTICS: History of Robots, Classifications, Various Fields of Robotics, Actuators, Sensors, Manipulators, End Effectors, Application Areas, Robot Programming Languages.

BASIC CONCEPTS: Definition and Origin of Robotics, Different Types of Robotics, Various Generations of Robots, Degrees of Freedom, Asimov's Laws of Robotics, Dynamic Stabilization of Robots.

UNIT - II

MANIPULATORS, ACTUATORS AND GRIPPERS: Construction of Manipulators, Manipulator Dynamics and Force Control, Electronic and Pneumatic Manipulator Control Circuits, End Effectors, Various Types of Grippers, Design Considerations.

UNIT - III

ROBOT KINEMATICS: Matrix Representation, Homogeneous Transformation, DH Representation of Standard Robots, Inverse Kinematics.

ROBOT DYNAMICS: Velocity Kinematics, Jacobian and Inverse Jacobian, Lagrangian Formulation, Euler's Lagrangian Formulation, Robot Equation of Motion.

UNIT - IV

TRAJECTORY PLANNING: Introduction, Path Vs Trajectory, Joint-Space Vs Cartesian, Space Descriptions, Basics of Trajectory Planning, Joint-Space Trajectory Planning, Cartesian-Space Trajectories. **APPLICATION OF ROBOTICS:** Architecture of Industrial Robotic Controllers, Robot Applications, Multiple Robots, Machine Interface.

UNIT - V

UNIT - VIII

CASE STUDIES: Robots in Manufacturing and Non- Manufacturing Applications, Robot Cell Design, Selection of Robot.

List of Text Books / References / Websites / Journals / Others

Text Books:

1. Saced B. Niku (2001), Introduction to Robotics Analysis, Systems, Applications, Prentice Hall of India / Pearson Education,NewDelhi,India .
2. Craig (2004), Introduction to Robotics Mechanics and Control, 2nd edition, Pearson Education,Boston.

Reference Books:

1. Mikell P. Weiss G. M, Nagel R .N, Odraj N. G(1996), Industrial Robotics, McGraw-Hill, India.
2. Ghosh (1998), Control in Robotics and Automation: Sensor Based Integration, Allied Publishers, India.
3. K. S. F Co(1991),RoboticsControl,Sensing,VisionandIntelligence,McGrawHillInternational,India.
4. R. D. Klafter, T. A. Chimielewski, M. Negin (1994), Robotic Engineering – An integrated Approach, Prentice Hall of India, India.
5. Mikell P. Groover, Mitchell Weiss, Roger N. Nagel, Nicholas G. Odrey(), Industrial Robotics Technology, Prentice Hall of India / Pearson Education, NewDelhi, India .

VARDHAMAN COLLEGE OF ENGINEERING
(AUTONOMOUS)

M. Tech. ES II SEMESTER

EMBEDDED NETWORK AND PROTOCOLS
(PROGRAM ELECTIVE – IV)

Course Code: **B4662**

L	T	P	C
3	0	0	3

UNIT - I

CAN BUS: Concept of bus access and arbitration, Error Processing and Management, Increase your word power, Historical context of CAN-Patents, Licence and Certification.

CAN PROTOCOL: *ISO 11898-1 Errors*: Their intrinsic properties, detection and processing, the rest of the Frame-CAN 2.0B.

UNIT - II

CAN PHYSICAL LAYER: Introduction, CAN bit, Nominal Bit Time-CAN and Signal Propagation-Bit Synchronization, Network Speed.

MEDIUM, IMPLEMENTATION AND PHYSICAL LAYERS OF CAN: The range of Media and types of coupling to the Network, High Speed CAN, Low Speed CAN, Optical Media, Electro Magnetic Media, Pollution and EMC Conformity.

UNIT – III

COMPONENTS, APPLICATIONS AND TOOLS FOR CAN: CAN Components, Applications, Application layers and development Tools for CAN.

FLEX RAY: Some General remarks, Event Triggered and Time Triggered Aspects, TTCAN-Towards High Speed, X-by-Wire and Redundant Systems-Flex Ray.

UNIT - IV

LIN: Introduction, Basic concept of LIN 2.0 Protocol, Cost and Market, Conformity of LIN, examples. **FAIL-SAFE SBC - GATEWAYS**: The Strategy and Principles of Re-use, Demo board-Gatways-Managing the Application Layers.

SAFE BY WIRE: History-Safe-by-Wire plus-Some Words of Technology.

UNIT - V

AUDIO-VIDEO BUSES: I2C Bus, D2B (Domestic digital) bus, MOST (Media oriented systems transport) bus - IEEE 1394 bus or 'FireWire'.

RF COMMUNICATION: Radio-frequency communication, internal Radio-frequency communication, external-Wireless Networks.

List of Text Books / References / Websites / Journals / Others

TEXT BOOKS:

1. Dominique Paret (2007), *Multiplexed Networks for Embedded Systems- CAN, LIN, Flexray, Safe-by-Wire,* John Wiley & Sons Ltd,Paris.

2. Jan Axelson(2005), *Embedded Ethernet and Internet Complete*, Penram publications,Madison.

REFERENCE BOOKS:

1. Glaf P. Feiffer, Andrew Ayre, Christian Keyold (2005), *Embedded networking with CAN and CAN open*, *Embedded System Academy,California*.

2. Gregory J. Pottie, William J. Kaiser (2005), *Principles of Embedded Networked Systems Design*, 2ndedition, Cambridge University Press,Newyork.

VARDHAMAN COLLEGE OF ENGINEERING
(AUTONOMOUS)

M. Tech. ES II SEMESTER

PYTHON PROGRAMMING LABORATORY

Course Code: **B4607**

L	T	P	C
0	0	3	2

LIST OF EXPERIMENTS:

1. Write a python program for implementing if/Else and Else If conditions.
2. Write a python program for implementing loops(for ,while loop)
3. Write a Python program that will take in a number from the user and print if it is positive, negative, or zero.
4. Write a Python program that asks the user for seven numbers. Then print the total, the number of positive entries, the number entries equal to zero, and the number of negative entries.
5. Create a program that asks the user for a temperature in Fahrenheit, and then prints the temperature in Celsius. Search the internet for the correct calculation
6. Create a program that will ask the user for the information needed to find the area of a trapezoid, and then print the area.
7. Write a single program in Python that will print the following:

10
11 12
13 14 15
16 17 18 19
20 21 22 23 24
25 26 27 28 29 30
31 32 33 34 35 36 37
38 39 40 41 42 43 44 45
46 47 48 49 50 51 52 53 54

8.Write code that will print the following:

1
1 2 1
12321
1234321
123454321
12345654321
1234567654321
123456787654321
1 2345678987654321

9.Write a function called min that will take three numbers and print the minimum number from entered numbers

10.Write code that will take a string from the user. Print the length of the string. Print the first letter of the string.

11.Write a function that will take two numbers as parameters (not as input from the user) and print their product (i.e. multiply them).

12.Write code to swap the values 15 and 14 list = [15,57,14,33,72,79,26,56,42,40]

13.Show how the following list of numbers is sorted, using the selection sort:

15	57	14	22	72	79	26	56	42	40

14. Show how the following list of numbers is sorted, using the insertion sort:

VARDHAMAN COLLEGE OF ENGINEERING

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M. Tech. ES II SEMESTER

EMBEDDED SYSTEM DESIGN USING PSOC LABORATORY

Course Code: **B4608**

L	T	P	C
0	0	3	2

75	53	36	2	60	18	65	64	55	82

LIST OF EXPERIMENTS:

1. Interface Seven Segment Display with PSoc Microcontroller.
2. Interface LEDs with PSoc Microcontroller.
3. Develop a program to perform Encryption and Decryption
4. Interface LCD with PSoc Microcontroller
5. Develop a program to read data from Sensor and to display data.
6. Serial Communication between Microcontrollers to PC vice versa
7. Interfacing Switches with PSoc Microcontroller.
8. Interface ADC with PSoc Microcontroller.
9. Port RTOS (µCos) to PSoc Board.
10. Simulate on elevator movement using RTOS on PSoc board.
11. Simulate coffee vending machine
12. Simulating Flash memory using PSOC.
13. Understanding serial communication between PC to PCin PSOC.
14. Designing of any automated system using PSOC.

Note: All the following experiments are expected to run by using PSOC

SYLLABI FOR
II YEAR III SEMESTER

VARDHAMAN COLLEGE OF ENGINEERING
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M. Tech. ES III SEMESTER

EMBEDDED CONTROL SYSTEMS
(PROGRAM ELECTIVE – V)

Course Code: **B4663**

L	T	P	C
3	0	0	3

UNIT - I

EMBEDDED SYSTEMS-BASIC CONCEPTS: What is an Embedded System?,The Main Architecture of Embedded Control Systems,Communication Networks in Embedded Systems,Multi-Tasking Embedded Control Systems,Planning Embedded System Development

INTRODUCTION INTO EMBEDDED CONTROL SYSTEM DESIGN: Requirements for Control System Design,Mathematical Model for Control,Control System's Characteristics,Performance Specifictions for Linear Systems

UNIT - II

SYSTEM IDENTIFICATION AND MODEL ORDER REDUCTION: Model Buliding and Model Structures,Input Signal Design for System Identification Experiment,Model Validation in Time and Frequency Domain,Model-order Reduction Methods,Nominal Plant and Plant Uncertainities,Practical Examples

UNIT - III

CLASSIC CONTROLLER DESIGN-PART I: Controller Design based on Pole-Zero Cancellation,Controller Design for Deadbeat Response, Controller Design using Root Locus Technique,PID Controller Design,The Coefficient Diagram Method,Validation for the Control System

CLASSIC CONTROLLER DESIGN-PART II: Controller Design for Systems with Time Delays, Controller Design for Disturbance Rejection,Disturbance Observers

UNIT - IV

FUNDAMENTALS OF ROBUST CONTROL: Review of Norms for Signals and Systems, Internal Stability,Unstructured Plant Uncertainties, Robust Stability, Robust Performance, Design for Robust Performance,Robust Controller Synthesis Problem

UNIT – V

ROBUST CONTROLLER DESIGN: Controller Design Using Robust Control Toolbox,Controller Design with **C**onstraint on the Control Signal,Robust Gain Scheduled Control,Control Alogirthm Implementation in Real-Time

EMBEDDED SAFETY LOOP DEVELOPMENT: Risk Assessment and Safety Levels,Classification of faults,Calculation of Probability of Failure on Demand,Software Testing and Validation,Memory Testing.

List of Text Books / References / Websites / Journals / Others

Text Books:

1. Alexandru Forrai*, Embedded Control System Design,A Model Based Approach, Springer*, India.

VARDHAMAN COLLEGE OF ENGINEERING
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M. Tech. ES III SEMESTER

EMBEDDED WIRELESS SENSOR NETWORKS
(PROGRAM ELECTIVE – V)

Course Code: **B4664**

L	T	P	C
3	0	0	3

UNIT I

WIRELESS SENSOR NETWORKS: Introduction to WSN-Challenges for WSNs , Why are sensor networks different?, Enabling technologies for Wireless Sensor Networks

SINGLE-NODE ARCHITECTURE -Hardware components, Energy consumption of sensor nodes, Operating systems and execution environments, Some examples of sensor nodes. UNIT II

NETWORK ARCHITECTURE: Sensor network scenarios, Optimization goals and figures of merit, Design principles for WSNs, Service interfaces of WSNs, Gateway concepts.

COMMUNICATION PROTOCOLS: Physical Layer introduction, Wireless channel and communication fundamentals, Physical layer and transceiver design considerations in WSNs. UNIT III

MAC PROTOCOLS: Fundamentals of (wireless) MAC protocols, Low duty cycle protocols and wakeup concepts, Contention-based protocols, Schedule-based protocols, The IEEE 802.15.4 MAC protocol.

LINK-LAYER PROTOCOLS: Fundamentals: tasks and requirements, Error control, Framing, Link management.
UNIT IV

TIME SYNCHRONIZATION: Introduction to the time synchronization problem, Protocols based on sender/receiver synchronization, Protocols based on receiver/receiver synchronization

TOPOLOGY CONTROL: Motivation and basic ideas, Controlling topology in flat networks – Power control, Hierarchical networks by dominating sets, Hierarchical networks by clustering, Combining hierarchical topologies and power control, Adaptive node activity.
UNIT V

ROUTING PROTOCOLS: The many faces of forwarding and routing, Gossiping and agent-based unicast forwarding, Energy-efficient unicast, Broadcast and multicast, Geographic routing, Mobile nodes.

TRANSPORT LAYER AND QUALITY OF SERVICE: The transport layer and QoS in wireless sensor networks, Coverage and deployment, Reliable data transport, Single packet delivery, Block delivery, Congestion control and rate control

ADVANCED APPLICATION SUPPORT : Advanced in-network processing, Security, Application-specific support.

List of Text Books / References / Websites / Journals / Others

TEXT BOOKS:

1. Holger karl, Andreas Willig(2005), “Protocols and architectures for wireless sensor networks”, John Wiley & Sons.

REFERENCE BOOKS:

1. Liljana Gavrilovska, Srdjan Krco, Veljko Milutinovic , Ivan Stojmenovic,Roman Trobec(2011), “Application and Multidisciplinary Aspects of Wireless Sensor Networks”, Springer-Verlag, London Limited.

2. Michel Banâtre, Pedro José Marrón, Anibal Ollero, Adam Wolisz(2008), ”Cooperating Embedded Systems and Wireless Sensor Networks “, John Wiley & Sons, Inc ..

3. Seetharaman Iyengar, Nandhan(2008), “Fundamentals of Sensor Network Programming Applications and Technology” , John Wiley & Sons.

VARDHAMAN COLLEGE OF ENGINEERING

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M. Tech. ES III SEMESTER

ELECTRONIC PRODUCT DESIGN AND RELIABILITY ENGINEERING
(PROGRAM ELECTIVE – V)

Course Code: **B4665**

L	T	P	C
3	0	0	3

UNIT - I

Introduction to Industrial Design (ID): General introduction, role of ID in the domain of industry, product innovation, designer's philosophy and role in product design, Product development tools and methods.

Product Design Methodology: Electronic product design and development, Methodology, creativity techniques, brain storming, documentation.

UNIT - II

Product Planning: Defining the task, scheduling the task, estimation of labor cost and amount of documentation.

Ergonomics & aesthetics: Ergonomics of electronics electronic use of ergonomics at work places and plat layouts, ergonomics of panel design, case study, Elements of aesthetics, aesthetics of control (ane) design.

UNIT - III

Visual Communication Techniques: Perspective, band sketching and rendering technique, elements of Engineering drawing, assembly drawing part drawing, exploded views.

Product Anatomy & Detailing: Layout design, structure design, standard and non standard structures, Industrials standards, Product detailing in sheet metal and plastics for ease of assembly, maintenance and aesthetics.

UNIT - IV

Product Manufacturing: Different manufacturing processes in sheet metal and plastics, product finishing, finishing methods like platting, anodization, spray painting , powder coating etc

UNIT - V

Reliable (Value) Engineering: Introduction to marketing, graphics & packing.

List of Text Books / References / Websites / Journals / Others

Text Books:

1. Peter Z. , "German Design Standard Vol 2", Reddot(2006)
2. Clarkson P. J, Coleman R. and Keates, S., "Inclusive Design, Design for the whole population", Springer Verlag Gmbh(2003)
3. Jordan P. W., "Designing Pleasurable Products: An Introduction to the New Human Factors." Taylor and Francis(2002)
4. Otto K. and Wood K., "Product design: Techniques in Reverse Engineering and New Product development ", Prentice Hall. (2001)
5. Cross N. "Engineering Design Methods: Strategies for Product Design", Willey.(2000)

Reference Books:

1. Cagan J. and Vogel C. M. (2007) Creating Breakthrough Products, “Innovation from Product Planning to Program Approval” . Pearson Education

2. Coats D. , “Watches Tell More than Time: Product Design, Information, Quest for elegance” McGraw Hill(2002)

3. Norman D. A. , “The design of everyday things, Basic Books.”(2002)

4. Chakrabarty D., “Indian Anthropometric Dimensions for Ergonomic Design Practice”, NID, Ahmedabad(1999).

5. Kelley T. and Littman J. “The Art of Innovation: Lessons in Creativity from Ideo, America's Leading Design Firm, Doubleday”, Ver: 4 November 2011 MI – PDN2524 Page 4 of 4 (2001)

6. E.J. McCormic, Human factors in engineering design, McGraw Hill 1976.

Journals:

1. Behaviour & Information Technology, Taylor & Francis

2. The Journal of Sustainable Product Design, Publisher: Springer

3. International Journal of Design; College of Design, National Taiwan University of Science and Technology, Taiwan.

4. Virtual & Physical Prototyping, Taylor & Francis

Internet Resources:

1. http://www.ulrich-eppinger.net/
2. http://www.npd-solutions.com
3. http://www.qfdi.org
4. http://www.cheshirehenbury.com/rapid/