VARDHAMAN COLLEGE OF ENGINEERING

(AUTONOMOUS)

(Permanently Affiliated to JNTUH, Approved by AICTE, New Delhi and Accredited by NBA)

Shamshabad - 501 218, Hyderabad

MASTER OF TECHNOLOGY
EMBEDDED SYSTEMS

ACADEMIC REGULATIONS, COURSE STRUCTURE AND SYLLABI FOR M.TECH - EMBEDDED SYSTEMS UNDER AUTONOMOUS STATUS FOR THE BATCHES ADMITTED FROM THE ACADEMIC YEAR 2011 - 12

Note: The regulations hereunder are subject to amendments as may be made by the Academic Council of the College from time to time. Any or all such amendments will be effective from such date and to such batches of candidates (including those already undergoing the program) as may be decided by the Academic Council.

PRELIMINARY DEFINITIONS AND NOMENCLATURES

- "Autonomous Institute / College" means an institute / college designated as autonomous institute / college by the Jawaharlal Nehru Technological University, Hyderabad (JNTUH), as per the JNTUH Autonomous College Statutes, 2011.
- "Academic Autonomy" means freedom to a College in all aspects of conducting its academic programs, granted by the University for promoting excellence.
- "Commission" means University Grants Commission.
- "AICTE" means All India Council for Technical Education.
- "University" the Jawaharlal Nehru Technological University, Hyderabad.
- "College" means Vardhaman College of Engineering, Hyderabad unless indicated otherwise by the context.
- "Program" means:
  Bachelor of Technology (B.Tech) degree program
  UG Degree Program: B.Tech
  PG degree Program: M.Tech
- "Branch" means specialization in a program like M.Tech degree program in Power Electronics and Electrical Drives.
- "Course" or "Subject" means a theory or practical subject, identified by its course – number and course-title, which is normally studied in a semester. For example, ABS11T01: Mathematics - I, ACS11T02: Data Structures through C, etc.
- T – Tutorial, P – Practical, D – Drawing, L - Theory, C - Credits

FOREWORD

The autonomy is conferred on Vardhaman College of Engineering by J N T University, Hyderabad based on its performance as well as future commitment and competency to impart quality education. It is a mark of its ability to function independently in accordance with the set norms of the monitoring bodies like UGC and AICTE. It reflects the confidence of the affiliating University in the autonomous institution to uphold and maintain standards it expects to deliver on its own behalf and thus awards degrees on behalf of the college. Thus, an autonomous institution is given the freedom to have its own **curriculum, examination system** and **monitoring mechanism**, independent of the affiliating University but under its observance.

Vardhaman College of Engineering is proud to win the credence of all the above bodies monitoring the quality in education and has gladly accepted the responsibility of sustaining, if not improving upon the standards and ethics for which it has been striving for more than a decade in reaching its present standing in the arena of contemporary technical education. As a follow up, statutory bodies like Academic Council and Boards of Studies are constituted with the guidance of the Governing Body of the College and recommendations of the JNTU Hyderabad to frame the regulations, course structure and syllabi under autonomous status.

The autonomous regulations, course structure and syllabi have been prepared after prolonged and detailed interaction with several expertise solicited from academics, industry and research, in accordance with the vision and mission of the college to order to produce a quality engineering graduate to the society.

All the faculty, parents and students are requested to go through all the rules and regulations carefully. Any clarifications needed are to be sought at appropriate time and with principal of the college, without presumptions, to avoid unwanted subsequent inconveniences and embarrassments. The Cooperation of all the stake holders is sought for the successful implementation of the autonomous system in the larger interests of the college and brighter prospects of engineering graduates.

PRINCIPAL

VARDHAMAN COLLEGE OF ENGINEERING

(Autonomous)

(Permanent Affiliation with JNTUH, Approved by AICTE, New Delhi and Accredited by NBA)

ACADEMIC REGULATIONS

M. Tech. Regular Two Year Post-Graduate Programme

(For the batches admitted from the academic year 2011–12)

For pursuing Two year degree program of study in Master of Technology (M.Tech.) offered by Vardhaman College of Engineering under Autonomous status and herein after referred to as VCE:

1. APPLICABILITY

All the rules specified herein, approved by the Academic Council, will be in force and applicable to students admitted from the academic year 2011-2012 onwards. Any reference to "College" in these rules and regulations stands for Vardhaman College of Engineering.

2. EXTENT

All the rules and regulations, specified herein after shall be read as a whole for the purpose of interpretation and as and when a doubt arises, the interpretation of the Chairman, Academic Council is final. As per the requirements of statutory bodies Principal, Vardhaman College of Engineering shall be the Chairman, Academic Council.

3. PROGRAMS OFFERED

Vardhaman College of Engineering, an autonomous college affiliated to JNTUH, offers the following M.Tech programmes of study leading to the award of M.Tech degree under the autonomous scheme.

S. No	M.Tech Courses	Intake
1	Computer Science and Engineering	36
2	Software Engineering	18
3	Digital Electronics and Communication Systems	36
4	Wireless and Mobile Communications	18
5	Power Electronics and Electrical Drives	18

4. ADMISSION

Admission into first year of Two Year M.Tech Program shall be made subject to the eligibility, qualifications and specialization as per the guidelines prescribed by the APSCHE and AICTE from time to time.

5. DURATION OF THE PROGRAMS

5.1 Normal Duration

M.Tech degree program extends over a period of two academic years leading to the Degree of Master of Technology (M.Tech) of the Jawaharlal Nehru Technology University, Hyderabad.

5.2 Maximum Duration

5.2.1 The maximum period within which a student must complete a full-time academic program is 4 years for M.Tech. If a student fails to complete the academic program within the maximum duration as specified above, he / she will be required to withdraw from the program.

5.2.3 The period is reckoned from the academic year in which the student is admitted first time into the degree programme.

6. SEMESTER STRUCTURE

The College shall follow semester pattern. An academic year shall consist of a first semester and a second semester and the summer term. Each semester shall be of 23 weeks duration and this period includes time for course work, examination preparation, and conduct of examinations. Each semester shall have a minimum of 90 working days. The academic calendar is shown in Table 1 is declared at the start of the semester. The duration for each semester shall be a minimum of 17 weeks of instruction.

Table 1: Academic Calendar

FIRST SEMESTER (23 weeks)	I Spell Instruction Period	: 9 weeks	19 weeks
	I Mid Examinations	: 1 week	
	II Spell Instruction Period	: 8 weeks	
	II Mid Examinations	: 1 Week	
	Preparation & Practical Examinations		2 weeks
	External Examinations		2 weeks
Semester Break			2 weeks
SECOND SEMESTER (23 weeks)	I Spell Instruction Period	: 9 weeks	19 weeks
	I Mid Examinations	: 1 week	
	II Spell Instruction Period	: 8 weeks	
	II Mid Examinations	: 1 Week	
	Preparation & Practical Examinations		2 weeks
	External Examinations		2 weeks
Summer Vacation			4 weeks
THIRD SEMESTER	Project Work Phase – I		18 Weeks
FOURTH SEMESTER	Project Work Phase – II		18 Weeks

7. CREDIT BASED SYSTEM

All the academic programs under autonomy are based on credit system. Credits are assigned based on the following norms:

7.1. The duration of each semester will normally be 23 weeks with 5 days a week. A working day shall have 6 periods each of 60 minutes duration.

- 1 credit per lecture period per week
- 2 credits for three (or more) period hours of practicals
- 2 credits for technical seminar
- 4 credits for comprehensive viva examination
- 18 credits for project work phase – I
- 22 credits for project work phase – II

7.2. The two year curriculum of any M.Tech programme of study shall have total of 88 credits. The exact requirements of credits for each course will be as recommended by the Board of Studies concerned and approved by the Academic Council.

7.3. For courses like technical seminar / comprehensive viva / Project Work Phases – I and II, where formal contact hours are not specified, credits are assigned based on the complexity of the work to be carried out.

8. METHOD OF EVALUATION

The performance of a student in each semester shall be evaluated subject-wise with a maximum of 100 marks each for theory and 100 marks for practical, on the basis of Internal Evaluation and End Semester Examination.

8.1 **Theory**

For all lecture based theory courses, the evaluation shall be for 40 marks through internal evaluation and 60 marks through external end semester examination of three hours duration.

8.1.1. Internal evaluation

For theory subjects, during the semester there shall be 2 midterm examinations. Each midterm examination consists of subjective test. The subjective test is for 40 marks, with duration of 2 hours. The Mid-Term Examination question paper shall be set with **six** questions out of which **four** are to be answered. All questions carry equal marks.

First midterm examination shall be conducted for I – IV units of syllabus and second midterm examination shall be conducted for the remaining portion.

The internal marks shall be computed as the average of the two internal evaluations, of two subjective tests.

8.1.2. External Evaluation

The question paper shall be set externally and valued both internally and externally. The external end semester examination question paper in theory subjects will be for a maximum of 60 marks to be answered in three hours duration. For End-Semester examination, the candidate has to answer any five out of eight questions. Each question carries 12 marks. Each theory course shall consist of eight units of syllabus.

8.2. **Practicals**

Practicals shall be evaluated for 100 marks, out of which 60 marks are for external examination and 40 marks are for internal evaluation. The 40 internal marks are distributed as 25 marks for day-to-day work and 15 marks for internal examination. The external end - examination shall be conducted by the teacher concerned and an external examiner from outside the college.

8.3. **Technical Seminar**

The seminar shall have two components, one chosen by the student from the course-work without repetition and approved by the faculty supervisor. The other component is suggested by the supervisor and can be a reproduction of the concept in any standard research paper or an extension of concept from earlier course work. A hard copy of the information on seminar topic in the form of a report is to be submitted for evaluation along with presentation. The presentation of the seminar topics shall be made before an internal evaluation committee comprising the Head of the Department or his/her nominee, seminar supervisor and a senior faculty of the department. The two components of the seminar are distributed between two halves of the semester and are evaluated for 50 marks each. The average of the two components shall be taken as the final score. A minimum of 50% of maximum marks shall be obtained to earn the corresponding credits.

8.4. **Comprehensive Viva**

The comprehensive Viva will be conducted by a committee comprising Head of the Department or his/her nominee, two senior faculty of the respective department and an external examiner from outside the college. This is aimed at assessing the student's understanding of various subjects studied during the entire program. The comprehensive viva shall be evaluated for 50 marks at the end of III semester. A minimum of 50% of maximum marks shall be obtained to earn the corresponding credits.

8.5. **Project Work**

The project work shall be evaluated for 200 marks out of which 50 marks for phase – I internal evaluation, 50 marks for phase – II internal evaluation and 100 marks for end semester evaluation. A minimum of 50% of marks on the aggregate in the internal evaluation and external end-evaluation taken together shall be obtained to earn the corresponding credits.

Every candidate is required to submit dissertation after taking up a topic approved by the Departmental Committee. The project work shall be spread over in III semester and in IV semester. The project work shall be somewhat innovative in nature, exploring the research bent of mind of the student.

The Departmental Committee (DC) consists of HOD, Supervisor and two senior experts in the department. The committee monitors the progress of Project Work. The DC is constituted by the Principal on the recommendations of the department Head.

Student shall register for the Project work with the approval of Departmental Committee in the III Semester and continue the work in the IV Semester too. The Departmental Committee (DC) shall monitor the progress of the project work. In III Semester, Phase – I of the Project Work is to be completed. A Student has to identify the topic of work, collect relevant Literature, preliminary data, implementation tools / methodologies etc., and perform a critical study and analysis of the problem identified. He shall submit status report in two different phases in addition to oral presentation before the Departmental Committee for evaluation and award of 50 internal marks at the end of Phase – I.

A candidate shall continue the Project Work in IV Semester (Phase – II) and submit a Project report at the end of Phase – II after approval of the Departmental Committee. During Phase – II, the student shall submit status report in two different phases, in addition to oral presentation before the DC. The DC shall evaluate the project for 50 internal marks based on the progress, presentations and quality of work.

A candidate shall be allowed to submit the dissertation only after passing all the courses of I and II semesters with the approval of Departmental Committee not earlier than **40 weeks** from the

date of registration of the project work and then take viva-voce examination. The viva-voce examination may be conducted once in three months for all the eligible candidates.

Three copies of the dissertation certified in the prescribed form by the supervisor and HOD shall be presented to the Department and one copy is to be submitted to the Controller of Examinations, VCE and one copy to be sent to the examiner.

The department shall submit a panel of three experts for a maximum of 5 students at a time. However, the examiners for conducting viva-voce examination shall be nominated by the Controller of Examinations, VCE. If the report of the examiner is favorable, viva-voce examination shall be conducted by a board consisting of the Supervisor, Head of the Department and the examiner who adjudicated the dissertation. The board shall jointly evaluate the project work for 100 marks. The candidates who fail in viva-voce examinations shall have to re-appear the viva-voce examination after three months. If he fails again in the second viva-voce examination, the candidate has to re-register for the Project Work.

If a candidate desires to change the topic of the project already chosen during Phase – I, he has to re-register for Project work with the approval of the DC and repeat Phases – I and II. Marks already earned in Phase – I stand cancelled.

9. ATTENDANCE REQUIREMENTS TO APPEAR FOR THE SEMESTER-END EXAMINATION

9.1. A student shall be eligible to appear for semester-end examinations if he acquires a minimum of 75% of attendance in aggregate of all the subjects in a semester.

9.2. Condonation of shortage of attendance in aggregate upto 10% (65% and above and below 75%) in each semester may be granted by the College Academic Committee.

9.3. Shortage of attendance below 65% in aggregate shall in no case be condoned.

9.4. Students whose shortage of attendance is not condoned in any semester are not eligible to take their semester-end examination of that class and their registration shall stand cancelled.

9.5. A student will not be promoted to the next semester unless he satisfies the attendance requirements of the current semester. The student may seek readmission for the semester when offered next. He will not be allowed to register for the subjects of the semester while he is in detention. A student detained due to shortage of attendance, will have to repeat that semester when offered next.

9.6. A stipulated fee shall be payable towards condonation of shortage of attendance to the College.

9.7. Attendance may also be condoned as per the recommendations of academic council for those who participate in prestigious sports, co-curricular and extra-curricular activities provided as per the Govt. of AP norms in vogue.

10. ACADEMIC REQUIREMENTS FOR PROMOTION / COMPLETION OF REGULAR M.TECH PROGRAMME OF STUDY

The following academic requirements have to be satisfied in addition to the attendance requirements for promotion / completion of regular M.Tech programme of study.

i. A student shall be deemed to have satisfied the minimum academic requirements for each theory, and practical, if he secures not less than 40% of marks in the semester-end examination and a minimum of 50% of marks in the sum of the internal evaluation and semester - end examination taken together.

ii. In case of technical seminar and comprehensive viva a student shall be deemed to have satisfied the minimum academic requirements and earned the credits allotted to each of them if he/she secures not less than 50% of marks.

iii. In case of project work, a student shall be deemed to have satisfied the minimum academic requirements and earned the credits allotted if he/she secures not less than 50% of marks on the aggregate in the internal evaluation and external end-evaluation taken together.

iv. A student shall register for all the 88 credits and earn all the 88 credits. Marks obtained in all the 88 credits shall be considered for the award of the class based on aggregate of marks.

v. A student who fails to earn 88 credits as indicated in the course structure within **FOUR** academic years from the year of their admission shall forfeit their seat in M.Tech programme and their admission stands cancelled.

viii. Students who are detained for want of attendance (or) who have not fulfilled academic requirements (or) who have failed after having undergone the course in earlier regulations (or) have discontinued and wish to continue the course are eligible for admission into the unfinished semester from the date of commencement of class work with the same (or) equivalent subjects as and when subjects are offered, and pursue the remaining course work with the academic regulations of the batch into which such students are readmitted. However, all such readmitted students shall earn all the credits of subjects they have pursued for completion of the course.

11. EVALUATION

Following procedure governs the evaluation.

11.1. Marks for components evaluated internally by the faculty should be submitted to the Controller of Examinations one week before the commencement of the semester-end examinations. The marks for the internal evaluation components will be added to the external evaluation marks secured in the semester-end examinations, to arrive at total marks for any subject in that semester.

11.2. Performance in all the courses is tabulated course-wise and will be scrutinized by the Examination Committee and moderation is applied if needed, based on the recommendations of moderation committee and course-wise marks lists are finalized.

11.3. Student-wise tabulation is done and student-wise memorandum of marks is generated which is issued to the student.

12. SUPPLEMENTARY EXAMINATION

Supplementary examinations for the odd semester shall be conducted with the regular examinations of even semester and vice versa, for those who appeared and failed in regular examinations. Such of the candidates writing supplementary examinations may have to write more than one examination per day.

13. RE-REGISTRATION FOR IMPROVEMENT OF INTERNAL

Following are the conditions to avail the benefit of improvement of internal marks.

13.1. The candidate should have completed the course work and obtained examinations results for I & II semesters.

13.2. A candidate shall be given one chance for a maximum of Three Theory subjects for Improvement of Internal evaluation marks for which the candidate has to re-register for the chosen subjects and fulfill the academic requirements.

13.3. For each subject, the candidate has to pay a fee equivalent to one third of the semester tuition fee and the amount is to be remitted in the form of D.D. in favour of the Principal, Vardhaman College of Engineering payable at Hyderabad along with the requisition through the concerned Head of the Department.

13.4. In the event of availing the Improvement of Internal evaluation marks, the internal evaluation marks as well as the End Examinations marks secured in the previous attempt(s) for the re-registered subjects stand cancelled.

14. PERSONAL VERIFICATION

Students shall be permitted for personal verification of the semester-end examination answer scripts within a stipulated period after payment of prescribed fee.

15. TRANSITORY REGULATIONS

Students who are detained for want of attendance (or) who have not fulfilled academic requirements (or) who have failed after having undergone the course in earlier regulations (or) have discontinued and wish to continue the course are eligible for admission into the unfinished semester from the date of commencement of class work with the same (or) equivalent subjects as and when subjects are offered, and pursue the remaining course work with the academic regulations of the batch into which such students are readmitted. A regular student has to satisfy all the eligibility requirements within the maximum stipulated period of four years for the award of M.Tech Degree.

16. TRANSCRIPTS

After successful completion of the entire programme of study, a transcript containing performance of all academic years will be issued as a final record. Transcripts will also be issued, if required, after payment of requisite fee. Partial transcript will also be issued upto any point of study to a student on request, after payment of requisite fee.

17. AWARD OF DEGREE

The degree will be conferred and awarded by Jawaharlal Nehru Technological University, Hyderabad on the recommendations of the Chairman, Academic Council.

17.1. Eligibility

A student shall be eligible for the award of M.Tech. Degree, if he fulfills all the following conditions:

i. Registered and successfully completed all the components prescribed in the programme of study to which he is admitted.

ii. Successfully acquired the minimum required credits as specified in the curriculum corresponding to the branch of study within the stipulated time.

iii. Obtained not less than 50% of marks (minimum requirement for declaring as passed).

iv. Has no dues to the college, hostel, and library etc. and to any other amenities provided by the College.

v. No disciplinary action is pending against him.

17.2. Award of Class

Declaration of Class is based on percentage of marks to be secured.

After a student has satisfied the requirement prescribed for the completion of the programme and is eligible for the award of M.Tech. Degree he shall be placed in one of the following four classes Shown in Table 4:

Table 4: Declaration of Class is based on percentage of marks to be secured

Class Awarded	% of marks to be secured	
First Class with Distinction	70% and above	From the aggregate marks secured for the 88 Credits.
First Class	Below 70% but not less than 60%	
Second Class	Below 60% but not less than 50%	
Fail	Below 50%	

Sometimes, it is necessary to provide equivalence of percentages and/or *Class* awarded with *Grade Point Average (GPA).* This shall be done by prescribing certain specific thresholds in averages for *Distinction, First Class and Second Class,* as in Table 5.

Table 5: Percentage Equivalence of *Grade Points* (For a 10-Point Scale)

Grade Point	Percentage of Marks / Class
5.75	50 (Second Class)
6.25	55
6.75	60 *(First Class)*
7.25	65
7.75	70 *(First Class with Distinction)*
8.25	75

18. REGISTRATION

Each student has to compulsorily register for course work at the beginning of each semester as per the schedule mentioned in the Academic Calendar. It is absolutely compulsory for the student to register for courses in time.

19. TERMINATION FROM THE PROGRAM

The admission of a student to the program may be terminated and the student is asked to leave the college in the following circumstances:

i. The student fails to satisfy the requirements of the program within the maximum period stipulated for that program.

ii. The student fails to satisfy the norms of discipline specified by the institute from time to time.

20. CURRICULUM

20.1. For each program being offered by the Institute, a Board of Studies (BOS) is constituted in accordance with AICTE / UGC / JNTUH statutes.

20.2. The BOS for a program is completely responsible for designing the curriculum once in three years for that program.

21. WITH-HOLDING OF RESULTS

If the candidate has not paid any dues to the college / if any case of indiscipline / malpractice is pending against him, the results of the candidate will be withheld. The issue of the degree is liable to be withheld in such cases.

22. GRIEVANCES REDRESSAL COMMITTEE

"Grievance and Redressal Committee" (General) constituted by the principal shall deal with all grievances pertaining to the academic / administrative / disciplinary matters. The composition of the complaints cum redressal committee shall be:

Headed by Senior Faculty member
Heads of all departments
A senior lady staff member from each department (if available)

The committee constituted shall submit a report to the principal of the college, the penalty to be imposed. The Principal upon receipt of the report from the committee shall, after giving an opportunity of being heard to the person complained against, submit the case with the committee's recommendation to the Governing Body of the college. The Governing Body shall confirm with or without modification the penalty recommended after duly following the prescribed procedure.

23. MALPRACTICE PREVENTION COMMITTEE

A malpractice prevention committee shall be constituted to examine and punish the students who does malpractice / behaves indiscipline in examinations. The committee shall consist of:

Principal
Subject expert of which the subject belongs to
Head of the department of which the student belongs to
The invigilator concerned
In-charge Examination branch of the college

The committee constituted shall conduct the meeting on the same day of examination or latest by next working day to the incidence and punish the student as per the guidelines prescribed by the J N T University, Hyderabad from time to time.

Any action on the part of candidate at the examination like trying to get undue advantage in the performance at examinations or trying to help another, or derive the same through unfair means is punishable according to the provisions contained hereunder. The involvement of the Staff, who are in charge of conducting examinations, valuing examination papers and preparing / keeping records of documents relating to the examinations in such acts (inclusive of providing incorrect or misleading information) that infringe upon the course of natural justice to one and all concerned at the examination shall be viewed seriously and recommended for award of appropriate punishment after thorough enquiry.

24. AMENDMENTS TO REGULATIONS

The Academic Council of Vardhaman College of Engineering reserves the right to revise, amend, or change the regulations, scheme of examinations, and / or syllabi or any other policy relevant to the needs of the society or industrial requirements etc., without prior notice.

25. STUDENTS' FEEDBACK

It is necessary for the Colleges to obtain feedback from students on their course work and various academic activities conducted. For this purpose, suitable feedback forms shall be devised by the College and the feedback obtained from the students regularly in confidence, by administering the feedback form in print or on-line in electronic form.

The feedback received from the students shall be discussed at various levels of decision making at the College and the changes/ improvements, if any, suggested shall be given due consideration for implementation.

26. GRADUATION DAY

The College shall have its own annual *Graduation Day* for the award of Degrees to students completing the prescribed academic requirements in each case, in consultation with the University and by following the provisions in the Statute.

The College shall institute Prizes and Awards to meritorious students, for being given away annually at the *Graduation Day.* This will greatly encourage the students to strive for excellence in their academic work.

27. AWARD OF A RANK UNDER AUTONOMOUS SCHEME

27.1. One (1) Merit Rank will be declared only for those students who have been directly admitted in VCE under Autonomous Regulations and complete the entire course in VCE only within the minimum possible prescribed time limit, i.e., 2 years for M.Tech.

27.2. A student shall be eligible for a merit rank at the time of award of degree in each branch of Master of Technology, provided the student has passed all subjects prescribed for the particular degree program in first attempt only.

27.5. Award of prizes, scholarships, or any other Honours shall be based on the rank secured by a candidate, consistent with the guidelines of the Donor, wherever applicable.

28. CONDUCT AND DISCIPLINE

28.1 Each student shall conduct himself / herself in a manner befitting his / her association with VCE.

28.2 He / she is expected not to indulge in any activity, which is likely to bring disrepute to the college.

28.3 He / she should show due respect and courtesy to the teachers, administrators, officers and employees of the college and maintain cordial relationships with fellow students.

28.4 Lack of courtesy and decorum unbecoming of a student (both inside and outside the college), wilful damage or removal of Institute's property or belongings of fellow students, disturbing others in their studies, adoption of unfair means during examinations, breach of rules and regulations of the Institute, noisy and unruly behaviour and similar other undesirable activities shall constitute violation of code of conduct for the student.

28.5 **Ragging in any form is strictly prohibited and is considered a serious offence. It will lead to the expulsion of the offender from the college.**

28.6 Violation of code of conduct shall invite disciplinary action which may include punishment such as reprimand, disciplinary probation, debarring from the examination, withdrawal of placement services, withholding of grades / degrees, cancellation of registration, etc., and even expulsion from the college.

28.7 Principal, based on the reports of the warden of Institute hostel, can reprimand, impose fine or take any other suitable measures against an inmate who violates either the code of conduct or rules and regulations pertaining to college hostel.

28.8 A student may be denied the award of degree / certificate even though he / she have satisfactorily completed all the academic requirements if the student is found guilty of offences warranting such an action.

28.9 Attendance is not given to the student during the suspension period.

29. OTHER ISSUES

The quality and standard of engineering professionals are closely linked with the level of the technical education system. As it is now recognized that these features are essential to develop the intellectual skills and knowledge of these professionals for being able to contribute to the society through productive and satisfying careers as *innovators, decision makers and/or leaders* in the global economy of the 21st century, it becomes necessary that certain improvements are introduced at different stages of their education system. These include:

i. Selective admission of students to a programme, so that merit and aptitude for the chosen technical branch or specialization are given due consideration.

ii. Faculty recruitment and orientation, so that qualified teachers trained in good teaching methods, technical leadership and students' motivation are available.

iii. Instructional/Laboratory facilities and related physical infrastructure, so that they are adequate and are at the contemporary level.

iv. Access to good library resources and Information & Communication Technology **(ICT)** facilities, to develop the student's *mind* effectively.

These requirements make it necessary for the College to introduce improvements like:

i. Teaching-learning process on modern lines, to provide *Add-On* Courses for *audit*/credit in a number of peripheral areas useful for students' self development.

ii. Life-long learning opportunities for faculty, students and alumni, to facilitate their dynamic interaction with the society, industries and the world of work.

iii. Generous use of ICT and other modern technologies in everyday activities.

30. GENERAL

Where the words "he", "him", "his", "himself" occur in the regulations, they include "she", "her", "herself".

Note: Failure to read and understand the regulations is not an excuse.

COURSE STRUCTURE

M. TECH – EMBEDDED SYSTEMS

REGULATIONS: VCE - R11

I SEMESTER							
Code	**Subject**	**Periods per Week**		**Credits**	**Scheme of Examination Maximum Marks**		
		L	**P**		**Internal**	**External**	**Total**
B1601	Advanced Data Structures and Algorithms	3	-	3	40	60	100
B1602	Microcontrollers for Embedded System Design	3	-	3	40	60	100
B1603	Embedded Real Time Operating Systems	3	-	3	40	60	100
B1414	DSP Processors and Architectures	3	-	3	40	60	100
PROFESSIONAL ELECTIVE - I		3	-	3	40	60	100
PROFESSIONAL ELECTIVE - II		3	-	3	40	60	100
B1609	Microcontrollers and Systems Lab	-	3	2	40	60	100
B1610	Technical Seminar	-	-	2	50	-	50
TOTAL		**18**	**03**	**22**	**330**	**420**	**750**
II SEMESTER							
Code	**Subject**	**Periods per week**		**Credits**	**Scheme of Examination Maximum Marks**		
		L	**P**		**Internal**	**External**	**Total**
B1611	Computer Architecture and Parallel processing	3	-	3	40	60	100
B1612	Embedded Software Design	3	-	3	40	60	100
B1407	CPLD and FPGA Architectures and Applications	3	-	3	40	60	100
B1417	Hardware Software Co-Design	3	-	3	40	60	100
PROFESSIONAL ELECTIVE - III		3	-	3	40	60	100
PROFESSIONAL ELECTIVE - IV		3	-	3	40	60	100
B1618	Embedded System Lab using PSOC	-	3	2	40	60	100
B1619	Technical Seminar	-	-	2	50	-	50
TOTAL		**18**	**03**	**22**	**330**	**420**	**750**
III SEMESTER							
Code	**Subject**	**Periods per week**		**Credits**	**Scheme of Examination Maximum Marks**		
		L	**P**		**Internal**	**External**	**Total**
B1620	Comprehensive Viva	-	-	4	-	50	50
B1621	Project Work Phase – I	-	-	18	50	-	50
TOTAL		**-**	**-**	**22**	**50**	**50**	**100**
IV SEMESTER							
Code	**Subject**	**Periods per week**		**Credits**	**Scheme of Examination Maximum Marks**		
		L	**P**		**Internal**	**External**	**Total**
B1622	Project Work Phase – II	-	-	22	50	100	150
TOTAL		**-**	**-**	**22**	**50**	**100**	**150**

M. TECH – EMBEDDED SYSTEMS

REGULATIONS: VCE - R11

ELECTIVES	
PROFESSIONAL ELECTIVE - I	
Code	**Subject**
B1604	Embedded Linux
B1605	Systems Programming
B1306	Optimization Techniques
PROFESSIONAL ELECTIVE - II	
B1606	Image and video processing
B1607	Soft Computing
B1608	System Modeling and Simulation
PROFESSIONAL ELECTIVE - III	
B1613	System On Chip Architecture
B1614	Embedded Network and protocols
B1615	Device Driver Development
PROFESSIONAL ELECTIVE - IV	
B1413	Network Security and Cryptography
B1616	Robotics and Automation
B1617	Application of MEMS

SYLLABI FOR I SEMESTER

M. Tech. ES I SEMESTER

ADVANCED DATA STRUCTURES AND ALGORITHMS

Course Code: **B1601**

L	P	C
3	-	3

UNIT - I

OVERVIEW OF DATA STRUCTURES: Review of arrays, stacks, queues, linked lists, linked stacks and linked queues, applications.

UNIT - II

ALGORITHM ANALYSIS: Efficiency of algorithms, apriori analysis, asymptotic notations, time complexity of an algorithm using o notation, polynomial vs. exponential algorithms, average, best and worst case complexities, analyzing recursive programs.

UNIT - III

TREES AND GRAPHS: Introduction, definition and basic terminologies of trees and binary trees, representation of trees and binary trees, binary tree traversals, threaded binary trees; Graphs basic concepts, representation and traversals.

UNIT - IV

BINARY SEARCH TREES, AVL TREES AND B -TREES: Introduction, *Binary Search Trees*: definition, operations and applications. *AVL Trees:* definition, operations and applications. *B- Trees:* definition, operations and applications.

UNIT - V

RED BLACK TREES, SPLAY TREES AND HASH TABLES: Red black trees, splay trees and its applications. *Hash tables:* introduction to hash tables, hash functions and its applications.

UNIT - VI

DIVIDE AND CONQUER AND GREEDY METHOD: General method, binary search, finding maximum and minimum, quick sort, merge sort, strassen's matrix multiplication. Greedy method, general method, minimum cost spanning trees, single source shortest path.

UNIT - VII

DYNAMIC PROGRAMMING: General method, all pairs shortest path, single source shortest path, 0/1 knapsack problem, reliability design, traveling sales person's problem.

UNIT - VIII

BACK TRACKING AND BRANCH AND BOUND: General method, 8 queen's problem, graph coloring. Branch and bound, the general method, LC search, control abstraction, bounding 0 / 1 knapsack problem.

TEXT BOOKS:

1. Ellis Horowitz, Sartaj Sahni, Sanguthevar Rajasekaran (2008), *Fundamentals of Computer Algorithms*, 2nd edition, University Press (India) Private Limited, India.
2. G. A. V. Pai (2009), *Data Structures and Algorithms*, Tata McGraw-Hill, New Delhi.

REFERENCE BOOKS:

1. D. Samanta (2003), *Classic Data Structures*, Prentice Hall of India Private Limited, New Delhi, India.
2. Aho, Hopcraft, Ullman (1998), *Design and Analysis of Computer Algorithms*, Pearson Education India, New Delhi, India.
3. Goodman, Hedetniemi (2002), *Introduction to the Design and Analysis of Algorithms*, Tata McGraw- Hill, New Delhi, India.
4. Adam Drozdek (2005), *Data Structures and Algorithms in C++,* 3rd Edition, Thomson Course Technology, New Delhi, India.

M. Tech. ES I SEMESTER

MICROCONTROLLERS FOR EMBEDDED SYSTEM DESIGN

Course Code: **B1602**

L	P	C
3	-	3

UNIT - I

8051 MICROCONTROLLERS: Microcontrollers and Embedded Systems, Overview of 8051 Family

8051 ASSEMBLY LANGUAGE PROGRAMMING: Inside the 8051,Introduction to 8051 Assembly Programming, Assembling and Running an 8051 Program, Program Counter and ROM Space in 8051,Data Types, Flag Bits and PSW Register,8051 Register Banks and Stack.

UNIT - II

INSTRUCTION SET: Loop and Jump Instructions, Call Instructions, Time Delay for various 8051 chips.

I/O PORT PROGRAMMING: 8051 I/O programming, I/O bit manipulation Programming.

UNIT - III

ADDRESSING MODES: Immediate and Register Addressing Modes, Accessing Memory using various Addressing Modes, Bit addresses for I/O and RAM, Extra 128-byte on-Chip RAM in 8052.

UNIT - IV

ARITHMETIC, LOGIC INSTRUCTIONS AND PROGRAMS: Arithmetic Instructions, Signed Number Concepts and Arithmetic Operations., Logic and Compare Instructions, Rotate Instruction and data Serialization, BCD, ASCII and Other Application Programs.

UNIT - V

EMBEDDED SYSTEM DESIGN: Overview, Design Challenge-Optimizing Design Metrics, Processor Technology, IC Techology, Design Technology, Trade-offs.

CUSTOM SINGLE-PURPOSE PROCESSORS: *Hardware:* Introduction, Combinational Logic, Sequential Logic, Custom Single-Purpose Processor Design, RT-Level Custom Single-Purpose Processor Design, Optimizing Custom Single-Purpose Processors.

UNIT - VI

GENERAL-PURPOSEPROCESSORS: SOFTWARE: Introduction, Basic Architecture, Operation, Programmers View, Development Environment, Application-Specific Instruction-Set Processors (ASIPs), Selecting a Microprocessor, General-Purpose Processor Design.

UNIT - VII

STANDARD SINGLE-PURPOSE PROCESSORS:PERIPHERALS: Introduction, Timers, Counters and Watchdog timers, UART, Pulse Width Modulators, LCD Controllers, Keypad Controllers, Stepper Motor Controllers, A/D Convertors, Real-Time Clocks.

UNIT - VIII

MEMORY: Introduction, Memory Write Ability and Storage Permanence, Common Memory Types, Composing memory, Memory Hierarchy and cache, Advanced RAM.

TEXT BOOKS:

1. Muhammad Ali Mazidi, Janice Gillispie Mazidi, Rolin D. Mckinlay (2009), *The 8051 Microcontroller and Embedded Systems*, 2nd edition, Pearson Education, New Delhi, India.
2. Frank Vahid, Tony Givargis (2005), *Embedded System Design: A Unified Hardware/Software Introduction*, Wiley Student Edition, New Delhi, India.

REFERENCE BOOKS:

1. Rajkamal (2008), *Embedded Systems- Architecture, Programming and Design*, 2nd edition, Tata McGraw- Hill, New Delhi, India.

M. Tech. ES I SEMESTER

EMBEDDED REAL TIME OPERATING SYSTEMS

Course Code: **B1603**

L	P	C
3	-	3

UNIT - I

INTRODUCTION: Introduction to UNIX, Overview of Commands, File I/O (open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec), Signals, Interprocess communication (pipes, fifos, message queues, semaphores, shared memory).

UNIT - II

REAL TIME SYSTEMS: Typical real time applications, Hard Vs. Soft real-time systems, *A Reference model of Real Time Systems:* Processors and Resources, Temporal Parameters of real Time Work load, Periodic task model precedence constraints and data dependency, functional parameters, Resource Parameters of jobs and parameters of resources.

UNIT - III

SCHEDULING: Commonly used Approaches to Real Time Scheduling Clock Driven, Weighted Round Robin, Priority Driven, Dynamic Vs State Systems, Effective release time and Deadlines, Offline Vs Online Scheduling.

UNIT - IV

INTER-PROCESS COMMUNICATION: Inter-process Communication and Synchronization of Processes, Tasks and Threads- Multiple Process in an Application, Problem of Sharing data by multiple tasks and routines, Inter-process communication.

UNIT - V

REAL TIME OPERATING SYSTEMS & PROGRAMMING TOOLS: Operating Systems Services, I/O Subsystems, RT and Embedded Systems OS, Interrupt Routine in RTOS Environment, Micro C/OS-II- Need of a well Tested & Debugged RTOs, Use of µCOS-II.

UNIT - VI

VX WORKS: Memory managements task state transition diagram, pre-emptive priority, Scheduling context switches- semaphore- Binary mutex, counting watch dugs, I/O system.

UNIT - VII

CASE STUDIES: Case Studies of programming with RTOS- Case Study of Automatic Chocolate Vending m/c using µCOS RTOS, case study of sending application Layer byte Streams on a TCP/IP network, Case Study of an Embedded System for a smart card.

UNIT - VIII

RTOS APPLICATION DOMAINS: RTOS for Image Processing - Embedded RTOS for voice over IP - RTOS for fault Tolerant Applications - RTOS for Control Systems.

TEXT BOOKS:

1. Jane W. S. Liu (2009), *Real Time Systems*, 8th edition, Pearson Education, New Delhi, India.
2. C. M. Krishna, Kang G. Shin (2010), *Real Time Systems*, 3rd edition, Tata McGraw-Hill, New Delhi, India.
3. Rajkamal (2008), *Embedded Systems- Architecture, Programming and Design*, 2nd edition, Tata McGraw-Hill, New Delhi, India.

REFERENCE BOOKS:

1. Tanenbaum (2008), *Distributed Operating Systems*, 5th edition, Pearson Education, New Delhi, India.
2. Raymond J. A. Bhur, Donald L. Bailey (1999), *An Introduction to Real Time Systems*, Prentice Hall of India, New Delhi, India.

M. Tech. ES I SEMESTER

DSP PROCESSORS AND ARCHITECTURES

Course Code: **B1414**

L	P	C
3	-	3

UNIT - I

INTORODUCTION TO DIGITAL SIGNAL PROCESING: Introduction, digital signal-processing system, the sampling process, discrete time sequences. discrete Fourier transform (DFT) and fast Fourier transform (FFT), linear time-invariant systems, digital filters, decimation and interpolation, analysis and design tool for DSP systems MATLAB, DSP using MATLAB.

UNIT - II

COMPUTATIONAL ACCURACY IN DSP IMPLEMENTATIONS: Number formats for signals and coefficients in DSP systems, dynamic range and precision, sources of error in DSP implementations, A/D conversion errors, DSP computational errors, D/A conversion errors, compensating filter.

UNIT - III

ARCHITECTURES FOR PROGRAMMABLE DSP DEVICES: Basic architectural features, DSP computational building blocks, bus architecture and memory, data addressing capabilities, address generation unit, programmability and program execution, speed issues, features for external interfacing.

UNIT - IV

EXECUTION CONTROL AND PIPELINING: Hardware looping, interrupts, stacks, relative branch support, pipelining and performance, pipeline depth, interlocking, branching effects, interrupt effects, and pipeline programming models.

UNIT - V

PROGRAMMABLE DIGITAL SIGNAL PROCESSORS : Commercial digital signal-processing devices, data addressing modes of TMS320C54XX DSPs, data addressing modes of TMS320C54XX processors, memory space of TMS320C54XX processors, program control, TMS320C54XX instructions and programming, on-chip peripherals, interrupts of TMS320C54XX processors, pipeline operation of TMS320C54XX processors.

UNIT - VI

IMPLEMENTATIONS OF BASIC DSP ALGORITHMS: The Q-notation, FIR filters, IIR filters, interpolation filters, decimation filters, PID controller, adaptive filters, 2-D signal processing.

UNIT - VII

IMPLEMENTATION OF FFT ALGORITHMS : An FFT algorithm for DFT computation, a Butterfly computation, overflow and scaling, bit-reversed index generation, an 8-Point FFT implementation on the TMS320C54XX, computation of the signal spectrum.

UNIT - VIII

INTERFACING MEMORY AND I/O PERIPHERALS TO PROGRAMMABLE DSP DEVICES: Memory space organization, external bus interfacing signals, memory interface, parallel I/O interface, programmed I/O, interrupts and I/O, direct memory access (DMA). a multichannel buffered serial port (McBSP), McBSP programming, a CODEC interface circuit, CODEC programming, a CODEC-DSP interface example.

TEXT BOOKS:

1. Avtar Singh, S. Srinivasan (2004), *Digital Signal Processing Implementations*, Thomson Publications, New Delhi, India.
2. Lapsleyetal. S (2000), *DSP Processor Fundamentals, Architectures & Features, S.* Chand & Co, New Delhi.

REFERENCE BOOKS:

1. B. Venkata Ramani, M. Bhaskar (2004), *Digital Signal Processors, Architecture, Programming and Applications*, Tata McGraw- Hill, New Delhi.
2. Jonatham Stein (2005), *Digital Signal Processing,* John Wiley, New Delhi.

M. Tech. ES I SEMESTER

EMBEDDED LINUX
(Professional Elective - I)

Course Code: **B1604**

L	P	C
3	-	3

UNIT - I

BASIC CONCEPTS: What Is an Embedded System? What Does Real-Time Mean? Implications of Open Source, Real Life and Embedded Linux Systems, Design and Implementation Methodology. Types of Hosts, Generic Architecture of an Embedded Linux System, System Startup, Types of Boot Configurations, System Memory Layout.

UNIT - II

BOOTING LINUX: Target BPR's, Linux Boot Process, The Linux Root File System, Creating the Root File System, Installing the TFTP Server, Installing Minicom, Booting the Embedded Planet, Booting the Bright star Engineering Media Engine target, Boot comparison.

UNIT - III

DEBUGGING: Introducing GDB, Local Debugging, Remote Debugging, Network Mounting the Root System.

UNIT - IV

INTERRUPTS: Linux Timing Sources, Measuring Interrupt Latency, Implementing the Race Timer.

UNIT - V

PARALLEL PORT INTERFACING: Control Using the Parallel Port, Standard Parallel Port Control with Port I/O, Standard Parallel Port Control Using PPDEV, Developing a Custom Device driver.

UNIT - VI

MEMORY INTERFACING: The Hardware Design Process, Developing Life Monitoring and Snowmaking Control for the Media-Engine.

UNIT - VII

ASYNCHRONOUS SERIAL COMMUNICATION INTERFACING: The project Trailblazer asynchronous serial hardware, Development Environment, Linux Serial Communication.

SYNCHRONOUS SERIAL COMMUNICATION INTERFACING: Temperature Sensing and Display, SPI Communication and the LM70, I2C Communication with the Philips Semiconductor.

UNIT - VIII

SYSTEM INTEGRATION: Integration Overview, Installing the System Integration Applications, Creating and Testing the Project Trailblazer Database, Developing the Target and CGI Integration Scripts, GUI Development, Real time Capabilities, Project Trailblazer Hardware.

TEXTBOOKS:

1. Dr. CraigHollabaugh (2004), *Embedded Linux: Hardware, Software and Interfacing*, 5th edition, Pearson Education, New Delhi, India.
2. Karim Yaghmour(2008), *Building Embedded Linux Systems*, 2nd edition, O'Reilly Media, New Delhi, India.

REFERENCE BOOKS:

1. J. Corbet, Rubini, Greg K. Hartman(2005), *Linux Device Drivers*, 3rd edition, O' Reilly Media, New Delhi, India.
2. P. Raghavan, Amol Lad, Sriram Neelakandan (2005), *Embedded Linux System Design and Development*, Auerbach Publications, CRC Press, USA.

M. Tech. ES I SEMESTER

SYSTEMS PROGRAMMING
(Professional Elective - I)

Course Code: **B1605**

L	P	C
3	-	3

UNIT - I

UNIX: Introduction to UNIX, Architecture, Basic Utilities, File Handling Utilities, File Permissions, Process Utilities, Disk Utilities, Networking Utilities, Backup Utilities, Filters and Text Processing and Manipulation Tools, GNU Tool Chain, Shell Responsibilities, Shell Programming, Shell Variables, Shell Script Examples.

UNIT - II

SYSTEM CALLS: Unix File Structure, Directories, Files and Devices, System Calls, Library Functions, Low Level File Access, Usage of Open, creat, read, write, close, seek, stat, fstat, ioctl, umask, dup and dup2,the Standard I/O (fopen, fopen, fclose, fflush, fseek, fgetc, getc, getchar, fputc, putc, putchar, fgets, gets).

UNIT - III

FORMATTED I/O AND DIRECTORY: Formatted I/O, Stream Errors, Streams and File Descriptors, File and Directory Maintenance (chmod, chown, unlink, link, symlink, mkdir, rmdir, chdir, getcwd), Directory Handling System Calls (opendir, readdir, closedir,rewinddir, seekdir, telldir).

UNIT - IV

PROCESS: Process, Process Structure, Starting New Process, Waiting for a Process, Zombie Process, Process Control, Process Identifiers, fork, Vfork, exit, wait, exec.

UNIT - V

SIGNALS: Signal functions, Unreliable Signals, Interrupted System Calls, kill and raise functions, alarm, pause functions, abort, system, sleep functions. Memory Management, Management of memory (malloc, free, realloc, calloc), File Locking (creating lock files, Locking regions, use of read/write locking, competing locks, other commands, deadlocks).

UNIT - VI

IPC: Pipe, Process Pipes, Pipe Call, Parent-Child Process, Named Pipes: FIFOs, Semaphores, Message Queues And Shared Memory and Applications of IPC.

UNIT - VII

NETWORK PROGRAMMING BASICS: Socket System Calls for Connection Oriented Protocol and Connectionless Protocol, Example-Client/Server Program, Simple TCP Socket Examples.

UNIT - VIII

DEVICE DRIVER PROGRAMMING: Introduction to Device Drivers, Role of Device Drivers, Splitting The Kernel, Classes of Devices and Modules, Security Issues, Version Numbering, Building and Running Modules Kernel Modules Vs. Applications, Compiling & Loading, Kernel Symbol Table, Preliminaries, Interaction and Shutdown, Module Parameters, Doing It In User Space, Kernel Module Programming.

TEXT BOOKS:

1. Sumitabha Das (2005), *Your UNIX: The Ultimate Guide*, 2nd edition, Tata McGraw-Hill, New Delhi, India.
2. W. R.Stevens, Stephen A. Rago (2005), *Advance Programming in the Unix Environment*, Addison-Wesley Professional, New Delhi, India.

REFERENCE BOOKS:

1. J. Corbet, Rubini, Greg K. Hartman (2005), *Linux Device Drivers,* 3rd edition, O' Reilly Media, USA.
2. W. Richard Stevens, Bill Fenner, Andrew M. Rudoff (2002), *UNIX Network Programming - The Sockets Networking API*, 3rd edition, Volume 1, PHI Learning Private Limited India, New Delhi.
3. Terrence Chan (1997)*, Unix system programming using C++,* Prentice Hall PTR, India.
4. Graham Glass, King Ables(2003), *Unix for programmers and users*, 3rd edition, Pearson Education, India.

M. Tech. ES I SEMESTER

OPTIMIZATION TECHNIQUES

(Professional Elective - I)

Course Code: **B1306**

L	P	C
3	-	3

UNIT - I

INTRODUCTION AND CLASSICAL OPTIMIZATION TECHNIQUES: Statement of an optimization problem, design vector, design constraints, constraint surface, objective function, objective function surfaces, classification of optimization problems.

UNIT - II

CLASSICAL OPTIMIZATION TECHNIQUES: Single variable optimization, multi variable optimization without constraints, necessary and sufficient conditions for minimum/maximum, multivariable optimization with equality constraints. Solution by method of Lagrange multipliers, multivariable optimization with inequality constraints, Kuhn – tucker conditions.

UNIT - III

LINEAR PROGRAMMING: Standard form of a linear programming problem, geometry of linear programming problems, definitions and theorems, solution of a system of linear simultaneous equations, pivotal reduction of a general system of equations, motivation to the simplex method, simplex algorithm.

UNIT - IV

TRANSPORTATION PROBLEM: Finding initial basic feasible solution by north - west corner rule, least cost method and Vogel's approximation method, testing for optimality of balanced transportation problems.

UNIT - V

UNCONSTRAINED NONLINEAR PROGRAMMING: One dimensional minimization methods, classification, Fibonacci method and quadratic interpolation method.

U**NIT - VI**

UNCONSTRAINED OPTIMIZATION TECHNIQUES: Univariate method, Powell's method and steepest descent method.

UNIT - VII

CONSTRAINED NONLINEAR PROGRAMMING: Characteristics of a constrained problem, classification, basic approach of penalty function method, basic approach of penalty function method, basic approaches of interior and exterior penalty function methods. Introduction to convex programming problem.

UNIT - VIII

DYNAMIC PROGRAMMING: Dynamic programming multistage decision processes, types, concept of sub optimization and the principle of optimality, computational procedure in dynamic programming, examples illustrating the calculus method of solution, examples illustrating the tabular method of solution.

TEXT BOOKS:

1. S. S. Rao (1998), *Engineering optimization*, 3rd edition, New Age International (P) Limited, New Delhi.
2. H. S. Kasene, K. D. Kumar (2004), *Introductory Operations Research,* Springer Private limited, India.

REFERENCE BOOKS:

1. K. V. Mital, C. Mohan(1996), *Optimization Methods in Operations Research and systems Analysis*, 3rd Edition, New Age International (P) Limited, New Delhi.
2. Dr. S. D. Sharma, H. A. Taha (1997), *Operations Research,* 6th Edition, Prentice Hall of India, New Delhi.
3. G. Hadley (1964), *Linear Programming,* 1st Edition, SIAM Publications, New Delhi.

M. Tech. ES I SEMESTER

IMAGE AND VIDEO PROCESSING

(Professional Elective - II)

Course Code: **B1606**

L	P	C
3	-	3

UNIT - I

FUNDAMENTALS OF IMAGE PROCESSING: Basic steps of Image Processing System Sampling and Quantization of an image, Basic relationship between pixels.

UNIT - II

IMAGE TRANSFORMS: 2D- Discrete Fourier Transform, Discrete Cosine Transform (DCT), Wavelet Transforms: Continuous Wavelet Transform, Discrete Wavelet Transforms.

UNIT - III

IMAGE ENHANCEMENT: Spatial domain methods: Histogram processing, Fundamentals of Spatial filtering, Smoothing spatial filters, Sharpening spatial filters. Frequency domain methods: Basics of filtering in frequency domain, image smoothing, image sharpening, Selective filtering.

UNIT - IV

IMAGE SEGMENTATION: Segmentation concepts, Point, Line and Edge Detection, Thresholding, Region Based segmentation.

UNIT - V

IMAGE COMPRESSION: Image compression fundamentals-Coding Redundancy, Spatial and Temporal redundancy, *Compression models:* Lossy and Lossless, Huffman coding, Arithmetic coding, LZW coding, Run length coding, Bit plane coding, Transform coding, Predictive coding, Wavelet coding, JPEG Standards.

UNIT - VI

BASIC STEPS OF VIDEO PROCESSING: Analog Video, Digital Video. Time-Varying Image Formation models: Three-Dimensional Motion Models, Geometric Image Formation, Photometric Image Formation, Sampling of Video signals, filtering operations.

UNIT - VII

2D MOTION ESTIMATION: Optical flow, General Methodologies, Pixel Based Motion Estimation, Block- Matching Algorithm, Mesh based Motion Estimation, Global Motion Estimation, Region based Motion Estimation, Multi resolution motion estimation, Waveform based coding, Block based transform coding, Predictive coding, Application of motion estimation in Video coding.

UNIT - VIII

VIDEO CODING USING TEMPORAL PREDICTION AND TRANSFORM CODING: Block-based video Hybrid Video Coding, Overlapped Blocked Motion Compensation, Coding parameter selection, Rate Control and loop filtering.

TEXT BOOKS:

1. Rafael C. Gonzaleze, Richard E. Woods (2007), *Digital Image Processing*, 3rd edition, Prentice Hall of India, New Delhi, India.
2. Ya-Qin Zhang, Jörn Ostermann (2002), *Video processing and communications*, 1st edition, Prentice Hall International, USA.

REFRENCE BOOKS:

1. A. Murat Tekalp (1995), *Digital Video Processing*, Prentice Hall PTR, USA.

M. Tech. ES I SEMESTER

SOFT COMPUTING
(Professional Elective - II)

Course Code: **B1607**

L	P	C
3	-	3

UNIT - I

INTRODUCTION TO ARTIFICIAL NEURAL NETWORKS: Introduction, Artificial Neural Networks, Historical Development of Neural Networks, Biological Neural Networks, Comparison Between Brain and the Computer, Comparison Between Artificial and Biological Neural Networks, Network Architecture, Setting the Weights, Activation Functions, Learning Methods.

UNIT - II

FUNDAMENTAL MODELS OF ARTIFICIAL NEURAL NETWORKS: Introduction, McCulloch – Pitts Neuron Model, Architecture, Learning Rules, Hebbian Learning Rule, Perceptron Learning Rule, Delta Learning Rule (Widrow-Hoff Rule or Least mean Square (LMS) rule, Competitive Learning Rule, Out Star Learning Rule, Boltzmann Learning, Memory Based Learning.

UNIT - III

PERCEPTRON NETWORKS: Introduction, Single Layer Perceptron Architecture- Algorithm, Application Procedure, Perception Algorithm for Several Output Classes, Perceptron Convergence Theorem, Brief Introduction to Multilayer Perceptron Networks.

FEED FORWARD NETWORKS: Back Propagation Network (BPN)- Generalized Delta Learning Rule(or) Back Propagation rule, Architecture, Training Algorithm, Selection of Parameters, Learning in Back Propagation, Application Algorithm , Local Minima and Global Minima, Merits and Demerits of Back Propagation Network, Applications, Radial Basis Function Network (RBFN), Architecture, Training Algorithm for an RBFN with Fixed Centers.

UNIT - IV

ADALINE AND MADALINE NETWORKS: Introduction, Adaline-Architecture, Algorithm, Application Algorithm, Madaline- Architecture, MRI Algorithm, MRII Algorithm.

UNIT - V

COUNTER PROPAGATION NETWORKS: Full Counter Propagation Network (Full CPN), Architecture, Training Phases of Full CPN, Training Algorithm, Application Procedure, Forward only Counter Propagation Network, Architecture, Training Algorithm, Application Procedure.

UNIT - VI

SELF ORGANIZING FEATURE MAP: Introduction, methods for Determining the Winner**,** Kohonen Self organizing Feature Maps (SOM).

ASSOCIATIVE MEMORY NETWORKS-I: Introduction, Algorithms for Pattern Association-Hebb Rule for Pattern Association, Delta Rule for Pattern Association, Extended Delta Rule,Hetero Associative Memory Neural Networks-Architecture, Application Algorithm.

UNIT - VII

ASSOCIATIVE MEMORY NETWORKS-II: Auto Associative Memory Network-Architecture, Training Algorithm, Iterative Auto Associative Net,Bi-directional Associative Memory-Architecture, Types of Bi-directional Associative Memory, Application Algorithm, Hamming Distance.

UNIT - VIII

APPLICATIONS OF NEURAL NETWORKS: Applications of Neural Networks in Bioinformatics, Neural Network in Health Care, Application in Pattern Recognition, Image Processing.

TEXTBOOKS:

1. S. N. Shivanandam, S. Sumati, S. N. Deepa(), *Introduction to Neural Networks Using MATLAB 6.0,* Tata McGraw-Hill, New Delhi, India.

REFERENCE BOOKS:

1. J. M. Zurada(2006), *Introduction to Artificial Neural Systems*, 3rd edition Jaico Publishers New Delhi.
2. Kishan Mehrotra, Chelkuri K. Mohan, Sanjay Ranka(1996), *Elements of Artificial Neural Networks*, Penram International, New Delhi.
3. Simon Haykin(1998) ,*Artificial Neural Network* , 2nd edition Prentice Hall of India, New Delhi.
4. B. Yegnanarayana(2004), *Artificial Neural Networks*, Prentice Hall of India, New Delhi.

M. Tech. ES I SEMESTER

SYSTEM MODELING AND SIMULATION

(Professional Elective - II)

Course Code: **B1608**

L	P	C
3	-	3

UNIT - I

BASIC SIMULATION MODELING: The Nature of Simulation, Systems, Models and Simulation, Discrete-Event Simulation, Time-Advance Mechanisms, Components and Organization of a Discrete-Event Simulation Model, Simulation of a Single-Server Queueing System ,Problem Statement, Intuitive Explanation, Simulation of an Inventory, Alternative Approaches to Modeling and Coding Simulations ,Steps in a Sound Simulation Study, Other Types of Simulation, Advantages, Disadvantages, and Pitfalls of Simulation.

UNIT - II

SIMULATION SOFTWARE: Introduction, Comparison of Simulation Packages with Programming Languages, Classification of Simulation Software, Desirable Software Features, General-Purpose Simulation Packages, Object-Oriented Simulation, Examples of Application-Oriented Simulation Packages.

UNIT - III

BUILDING SIMULATION MODELS: Guidelines for determining levels of model detail, Techniques for increasing model validity and credibility.

UNIT - IV

MODELING TIME DRIVEN SYSTEMS: Modeling input signals, delays, System Integration, Linear Systems, Motion Control models, numerical experimentation.

UNIT - V

EXOGENEOUS SIGNALS AND EVENTS: Disturbance signals, state machines, Petri nets and analysis, System encapsulation.

UNIT - VI

MARKOV PROCESS: Probabilistic systems, Discrete Time Markov processes, Random walks, Poisson processes, the exponential distribution, simulating a poison process, Continuous - Time Markov processes.

UNIT - VII

EVENT DRIVEN MODELS: Simulation diagrams, Queing theory, simulating queing systems, Types of Queues, Multiple servers.

UNIT - VIII

SYSTEM OPTIMIZATION: System identification, Searches, Alpha/beta trackers, multidimensional optimization, modeling and simulation methodology.

TEXT BOOKS:

1. Frank L. Severance (2009), *System Modeling and Simulation - An introduction*, John Wiley & Sons, New Delhi.
2. Averill M. Law, W. David Kelton (1982), *Simulation Modeling and Analysis*, 3rd edition, Tata McGraw-Hill, New Delhi, India.

REFERENCE BOOKS:

1. Gordan Gephery (2005), Systems *Simulation*, Prentice Hall of India, New Delhi, India.

M. Tech. ES I SEMESTER

MICROCONTROLLERS AND SYSTEMS LAB

Course Code: **B1609**

L	P	C
-	3	2

LIST OF EXPERIMENTS:

1. Programming using Arithmetic, logical and bit manipulations instructions of 8051.
2. Develop and execute the program to interface Keyboard to the 8051 Microcontroller.
3. Develop and execute the program to interface DAC to the 8051 Microcontroller.
4. Establish Serial communication between the 8051 Microcontroller and PC.
5. Interface 8279 (Key Board and Display Controller) with 8051 Microcontroller.
6. Program to verify Timer/Counter in 8051 Microcontroller.
7. Interrupt programming in 8051 Microcontroller.
8. To develop and execute the program for UART operation in 8051.
9. Program to verify counter in 8051.
10. Develop and execute the program for synchronous transmitter.
11. Communication between two PC's using ARM processor.
12. Verify Asynchronous multiplier using ARM processor.
13. Verify Asynchronous division using ARM processor.
14. Program to understand serial communication among PC/8051/PC.

Note: All these experiments are expected to run based on ARM processor

SYLLABI FOR II SEMESTER

M. Tech. ES II SEMESTER

COMPUTER ARCHITECTURE AND PARALLEL PROCESSING

Course Code: **B1611**

L	P	C
3	-	3

UNIT - I

INTRODUCTION TO PARALLEL PROCESSING: Evolution of Computer Systems, Parallelism in Uniprocessor Systems, Parallel Computer Structures, Architectural Classification Schemes, Parallel Processing Applications.

UNIT - II

MEMORY AND INPUT-OUTPUT SUBSYSTEMS: Hierarchical Memory Structure, Virtual Memory System, Memory Allocation and Management, Cache Memories and Management, Input-output Subsystems.

UNIT - III

PRINCIPLES OF PIPELINING: Pipelining: An Overlapped Parallelism-Principles of Linear Pipelining, Classification of Pipeline Processors, General Pipelines and Reservation Tables, Instruction and Arithmetic Pipelines-Design of pipelined Instruction Units, Arithmetic Pipelines Design Examples, Multifunction and Array Pipelines.

UNIT - IV

VECTOR PROCESSING: Principles of Designing Pipelined Processors-Instruction Prefetch and Branch handling, Data Buffering and Busing Structures, Internal Forwarding and register Tagging, Hazard Detection and Resolution, Job Sequencing and Collision Prevention, Dynamic Pipelines and Reconfigurability, Vector Processing Requirements-Characteristics of Vector Processing, Multiple Vector Task Dispatching, Pipelined Vector Processing Methods.

UNIT - **V**

PIPELINE COMPUTERS: The Space of pipelined Computers-Vector Supercomputers, Scientific Attached Processors, Early vector Processors-Architectures of Star-100 and TI-ASC,Vector Processing in Streaming Mode, Scientific Attached Processors-Architecture of AP-120B,Back-end vector computations,FPS-164,IBM 3828 and Datawest MATP.

1.

UNIT - VI

VECTORIZATION METHODS: Recent Vector Processors-Architecture of Cray-1,Pipeline Chaining and Vector loops, Architecture of Cyber-205,Vector processing in Cyber-205 and CDC-NASF, Fujitsu VP-200 and Special features, Vectorization and Optimization Methods-Language features in Vector Processing, Design of vectorizing Compilers, Optimization of Vector Operations, Performance Evaluation of Pipelined Operations Computers.

UNIT - VII

MULTIPROCESSOR ARCHITECTURE: Functional Structures-Loosely coupled Multiprocessors, Tightly Coupled Multiprocessors, Processor Characteristics for Multiprocessing, Interconnection Networks-Time Shared or Common Buses, Crossbar Switch and Multiport Memories, Multistage Networks for Multiprocessors, Performance of Interconnection Networks.

UNIT - VIII

MULTIPROCESSOR PROGRAMMING: Parallel Memory Organizations-Interleaved Memory Configurations, Performance Tradeoffs in Memory Organizations,Multicache Problems and Solutions, Multiprocessor Operating Systems-Classification of Multiprocessor Operating Systems, Software requirements for Multiprocessors, Operating System Requirements, Exploiting Concurrency for Multiprocessing-Language Features to Exploit parallelism, Detection of parallelism in Programs, Program and Algorithm Restructing.

TEXT BOOKS:

1. Kai Hwang, Faye A. Briggs (1984), *Computer Architecture and Parallel Processing*, Tata McGraw-Hill International Edition, New Delhi.

REFERENCE BOOKS:

1. Kai Hwang (2003), *Advanced Computer Architecture,* Tata McGraw-Hill, New Delhi.

M. Tech. ES II SEMESTER

EMBEDDED SOFTWARE DESIGN

Course Code: **B1612**

L	P	C
3	-	3

UNIT - I

PENTIUM PROCESSOR: Introduction to the Pentium microprocessor, special Pentium registers, Pentium, memory management.

UNIT - II

EMBEDDED DESIGN LIFE CYCLE: Introduction, Product Specification, Hardware/software partitioning, Iteration and Implementation, Detailed hardware and software design, Hardware/Software integration, Product Testing and Release, Maintaining and upgrading existing products.

UNIT - III

SELECTION PROCESS: Packaging the Silicon, Adequate Performance, RTOS Availability, Tool chain Availability, Other issues in the Selection process, Partitioning Decision: Hardware/Software Duality, Hardware Trends, ASICs and Revision Costs.

UNIT - IV

DEVELOPMENT ENVIRONMENT: The Execution Environment, Memory Organization, System Startup. Special Software Techniques: Manipulating the Hardware, Interrupts and Interrupt service Routines (ISRs), Watchdog Times, Flash Memory, Design Methodology.

UNIT - V

BASIC TOOL SET: Host - Based Debugging, Remote Debuggers and Debug Kernels, ROM Emulator, Logic Analyzer.

UNIT - VI

BDM: Background Debug Mode, Joint Test Action Group (JTAG) and Nexus. ICE – Integrated Solution: Bullet Proof Run Control, Real time trac, Hardware Break points, Overlay memory, Timing Constrains, Usage Issue, Setting the Trigger. Testing: Why Test? When to Test? Which Test? When to Stop? Choosing Test cases, Testing Embedded Software, Performance Testing Maintenance and Testing, The Future.

UNIT - VII

WRITING SOFTWARE FOR EMBEDDED SYSTEMS: The compilation Process, Native Versus Cross-Compilers, Runtime Libraries, Writing a Library, Using alternative Libraries, using a standard Library, Porting Kernels, C extensions for Embedded Systems, Downloading. Emulation and debugging techniques.

UNIT - VIII

BUFFERING AND OTHER DATA STRUCTURES: What is a buffer? Linear Buffers, Directional Buffers, Double Buffering, Buffer Exchange, Linked Lists, FIFOs, Circular Buffers, Buffer Under run and Overrun, Allocating Buffer Memory, Memory Leakage. Memory and Performance Trade-offs.

TEXT BOOKS:

1. Arnold S Burger (2002), *Embedded Systems Design: Introduction to Processes, Tools, Techniques*, CMP Books, USA.
2. Steave Heath (2003), *Embedded Systems Design*, 2nd edition, Newness Publications, Burlington, USA.

REFERENCE BOOKS:

1. Andrew N. Sloss, Dominic Symes, Cheris Wright(2004), ARM *Systems Developers Guide Designing and Optimizing System Software*, Elsevier Publication, San Fransisco, USA.
2. Daniel P. Bovet, Marco Cesati (2005), *Understanding the Linux Kernel*, 3rd edition, O'Reilly Media, USA.

M. Tech. ES II SEMESTER

CPLD AND FPGA ARCHITECTURES AND APPLICATIONS

Course Code: **B1407**

L	P	C
3	-	3

UNIT - I

FPGA BASED SYSTEMS: Introduction, basic concepts, digital design and FPGAs, FPGA based system design.

UNIT - II

FPGA FABRICS: Introduction, FPGA architectures, SRAM based FPGAs, permanently programmed FPGAs.

UNIT - III

FPGA FABRICS II: Chip input/output, circuit design of FPGA fabrics, architecture of FPGA fabrics.

UNIT - IV

COMBINATIONAL LOGIC: Logic design process, combinational network delay, power and energy optimization and arithmetic logic.

UNIT - V

LOGIC IMPLEMENTATION USING FPGAs: Syntax directed translation, logic implementation by macro, logic synthesis, technology independent and dependent logic optimizations, physical design for FPGAs, logic design process revisited.

UNIT - VI

SEQUENTIAL MACHINES: Introduction, sequential machine design process, sequential design styles, rules for clocking, performance analysis.

UNIT - VII

INTRODUCTION TO PLDS: Introduction to PLDs, programmable sum-of-products arrays, PAL fuse matrix and, combinational outputs, PAL outputs with programmable polarity, PAL devices with programmable polarity, universal PAL and generic array logic.

UNIT - VIII

CASE STUDIES: Case studies Xilinx XC4000 and ALTERA's FLEX 8000.

TEXT BOOKS:

1. Wayne Wolf (2004), *FPGA Based System Design*, Pearson Education, New Delhi.
2. Robert Dueck (2000), *Digital design With CPLD Applications and VHDL,* Thomson Learning, USA.

REFERENCE BOOKS:

1. Vikram Arkalgud (2011), *VLSI Design: A Practical Guide for FPGA and ASIC Implementations*, Springer Science, USA.
2. Leo Chartrand (2003), *Advanced Digital Systems: Experiments & Concepts With CPLD's*, Thomson Learning, USA.

M. Tech. ES II SEMESTER

HARDWARE SOFTWARE CO-DESIGN

Course Code: **B1417**

L	P	C
3	-	3

UNIT - I

CO DESIGN ISSUES: Co- design models, architectures, languages, and a generic co-design methodology.

UNIT - II

CO SYNTHESIS ALGORITHMS: Hardware software synthesis algorithms, hardware – software partitioning distributed system co-synthesis.

UNIT - III

PROTOTYPING AND EMULATION: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure.

UNIT - IV

TARGET ARCHITECTURES: Architecture specialization techniques, system communication infrastructure, target architecture and application system classes, architecture for control dominated systems (8051-architectures for high performance control), architecture for data dominated systems (ADSP21060, TMS320C60), mixed systems.

UNIT - V

COMPILATION TECHNIQUES AND TOOLS FOR EMBEDDED PROCESSOR ARCHITECTURES: Modern embedded architectures, embedded software development needs, compilation technologies practical consideration in a compiler development environment.

UNIT - VI

DESIGN SPECIFICATION AND VERIFICATION: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification.

UNIT - VII

LANGUAGES FOR SYSTEM LEVEL SPECIFICATION AND DESIGN-I: System – level specification, design representation for system level synthesis, system level specification languages.

UNIT - VIII

LANGUAGES FOR SYSTEM LEVEL SPECIFICATION AND DESIGN-II: Heterogeneous specifications and multi language co-simulation the Cosyma system and Lycos system.

TEXT BOOKS:

1. Jorgen Staunstrup, Wayne Hendrix Wolf (2002), *Hardware / software co- design Principles and Practice*, kluwer academic publishers, USA.

REFERENCE BOOKS:

1. Patrick R. Schaumont (2010), *A Practical Introduction to Hardware/Software Do-design*, Springer.
2. Giovanni De Micheli, Mariagiovanna Sami (1996), *Hardware/Software Co-design*, Kluwer Academic.

M. Tech. ES II SEMESTER

SYSTEM ON CHIP ARCHITECTURE

(Professional Elective - III)

Course Code: **B1613**

L	P	C
3	-	3

UNIT - I

INTRODUCTION TO PROCESSOR DESIGN: Abstraction in Hardware Design, MUO a Simple processor, Processor Design Trade Off, Design For Low Power Consumption.

UNIT - II

ARM PROCESSOR AS SYSTEM–ON-CHIP: Acron RISC Machine-Architecture Inherence-Arm Programming Model-ARM Development Tools-3 and 5 Stage Pipeline ARM Organization-ARM Instruction Execution and Implementation-ARM Co-Processor Interface.

UNIT - III

ARM ASSEMBLY LANGUAGE PROGRAMMING: ARM Instruction Types, Data Transfer, Data processing and Control Flow Instructions, ARM Instruction Set, Co-Processor Instructions.

UNIT - IV

ARCHITECTURE SUPPORT FOR HIGH LEVEL LANGUAGE: Data Types, Abstraction in Software Design, Expressions, Loops, Functions and Procedures, Conditional Statements, Use of Memory.

UNIT - V

MEMORY HIERARCHY: Memory Size and Speed On-Chip, Memory-Caches, Cache Design, An example Memory Management.

UNIT - VI

ARCHITECTURAL SUPPORT FOR SYSTEM DEVELOPMENT: Advanced Microcontroller Bus Architecture (AMBA), ARM Memory Interface, ARM Reference Peripheral Specification, Hardware System Prototyping Tools, Armulator, Debug Architecture.

UNIT - VII

ARCHITECTURAL SUPPORT FOR OPERATING SYSTEMS: An Introduction to Operating Systems, ARM System Control Co Processor-CP15 Protection Unit Registers-ARM Protection Unit-CP15MMU Registers-ARM MMU Architecture-Synchronization-Context Switching Input and Output.

UNIT - VIII

ARM CPU CORES: The ARM710T, ARM720T and ARM740T, the ARM810, the Strong ARM SA-110.

TEXT BOOKS:

1. Steve Furber (2000), *ARM System on Chip Architecture*, 2nd edition, Addison Wesley Professional, USA.
2. Ricardo Reis (2004), *Design of System on a Chip: Devices and Components*, 1st edition, Springer, USA.

REFERENCE BOOKS:

1. Jason Andrews (2004), *CoVerification of Hardware and Software for ARM System on Chip Design Embedded Technology*, Newness Publications, USA.
2. Prakash Rashinkar, Peter Paterson, Leena Sing L (2001), *System on Chip Verification–Methodologies and Techniques*, Kluwer Academic Publishers, USA.

M. Tech. ES II SEMESTER

EMBEDDED NETWORK AND PROTOCOLS

(Professional Elective - III)

Course Code: **B1614**

L	P	C
3	-	3

UNIT - I

CAN BUS: Concept of bus access and arbitration, Error Processing and Management, Increase your word power, Historical context of CAN-Patents, Licence and Certification.

CAN PROTOCOL: *ISO 11898-1 Errors*: Their intrinsic properties, detection and processing, the rest of the Frame-CAN 2.0B.

UNIT - II

CAN PHYSICAL LAYER: Introduction, CAN bit, Nominal Bit Time-CAN and Signal Propagation-Bit Synchronization, Network Speed.

UNIT - III

MEDIUM, IMPLEMENTATION AND PHYSICAL LAYERS OF CAN: The range of Media and types of coupling to the Network, High Speed CAN, Low Speed CAN, Optical Media, Electro Magnetic Media, Pollution and EMC Conformity.

UNIT - IV

COMPONENTS, APPLICATIONS AND TOOLS FOR CAN: CAN Components, Applications, Application layers and development Tools for CAN.

FLEX RAY: Some General remarks, Event Triggered and Time Triggered Aspects, TTCAN-Towards High Speed, X-by-Wire and Redundant Systems-Flex Ray.

UNIT - V

LIN: Introduction, Basic concept of LIN 2.0 Protocol, Cost and Market, Conformity of LIN, examples.

UNIT - VI

FAIL-SAFE SBC -GATEWAYS: The Strategy and Principles of Re-use, Demo board-Gatways-Managing the Application Layers.

SAFE BY WIRE: History-Safe-by-Wire plus-Some Words of Technology.

UNIT - VII

AUDIO-VIDEO BUSES: I2C Bus, D2B (Domestic digital) bus, MOST (Media oriented systems transport) bus - IEEE 1394 bus or 'FireWire'.

UNIT - VIII

RF COMMUNICATION: Radio-frequency communication, internal Radio-frequency communication, external-Wireless Networks.

TEXT BOOKS:

1. Dominique Paret (2007), *Multiplexed Networks for Embedded Systems- CAN, LIN, Flexray, Safe-by-Wire,* John Wiley & Sons Ltd, USA.
2. Jan Axelson (2005), *Embedded Ethernet and Internet Complete*, Penram publications, USA.

REFERENCE BOOKS:

1. Glaf P. Feiffer, Andrew Ayre, Christian Keyold (2005), *Embedded networking with CAN and CAN open*, *Embedded System Academy*, CA, USA.
2. Gregory J. Pottie, William J. Kaiser (2005), *Principles of Embedded Networked Systems Design*, 2nd edition, Cambridge University Press, New York, USA.

M. Tech. ES II SEMESTER

DEVICE DRIVER DEVELOPMENT

(Professional Elective - III)

Course Code: **B1615**

L	P	C
3	-	3

UNIT - I

INTRODUCTION: The Role of the Device Driver, Splitting the Kernel, Classes of Devices and Modules, Security Issues, Kernel Modules Versus Applications, Compiling and Loading, The Kernel Symbol Table, Preliminaries, Initialization and Shutdown, Module Parameters.

UNIT - II

CHAR DRIVERS AND DEBUGGING TECHNIQUES: The Design of scull, Major and Minor Numbers, Some Important Data Structures, Char Device Registration, open and release, scull's Memory Usage, read and write, Playing with the New Devices, Debugging Support in the Kernel, Debugging by Printing, Debugging by Querying, Debugging by Watching, Debugging System Faults, Debuggers and Related Tools.

UNIT - III

CONCURRENCY AND RACE CONDITIONS: Pitfalls in scull, Concurrency and Its Management, Semaphores and Mutexes, Completions, Spinlocks Locking Traps, Alternatives to Locking.

UNIT - IV

ADVANCED CHAR DRIVER OPERATIONS: IOCTL, Blocking I/O, poll and select, Asynchronous Notification, Seeking a Device, Access Control on a Device File, Measuring Time Lapses, Knowing the Current Time, Delaying Execution, Kernel Timers, Task lets.

UNIT - V

MEMORY ALLOCATION: The Real Story of Kmalloc, Look aside Caches, get_free_page and Friends, Vmalloc and Friends, Per-CPU Variables, Obtaining Large Buffers.

UNIT - VI

COMMUNICATING WITH HARDWARE: I/O Ports and I/O Memory, Using I/O Ports, An I/O Port Example, Using I/O Memory.

UNIT - VII

INTERRUPT HANDLING: Preparing the Parallel Port, Installing an Interrupt Handler, Implementing a Handler, Top and Bottom Halves, Interrupt Sharing, Interrupt-Driven I/O.

UNIT - VIII

DATA TYPES IN THE KERNEL: Use of Standard C Types, Assigning an Explicit Size to Data Items, Interface-Specific Types, Other Portability Issues, Linked Lists, A Simple case study.

TEXT BOOKS:

1. Jonathan Corbet, Alessandro Rubini, Greg Kroah-Hartman (2005), *Linux Device Drivers*, 3rd edition, O'Reilly, Publishers, CA, USA.
2. Sreekrishnan Venkateswaran(2008), *Essential Linux Device Drivers*, Prentice Hall Publishers, USA.

REFERENCE BOOKS:

1. Robert Love (2010), *Linux Kernel Development*, 3rd edition, Addison Wesley, USA.
2. Christopher Hallinan (2010), *Embedded Linux Primer: A Practical Real-World Approach*, 2nd edition, Prentice Hall Publishers, USA.

M. Tech. ES II SEMESTER

NETWORK SECURITY AND CRYPTOGRAPHY

(Professional Elective - IV)

Course Code: **B1413**

L	P	C
3	-	3

UNIT - I

INTRODUCTION SECURITY ATTACKS: Interruption, interception, modification and fabrication.

SECURITY SERVICES: Confidentiality, authentication, integrity, non repudiation, access control and availability.

SECURITY MECHANISMS: A model for internetwork security, internet standards and RFCs, conventional encryption principles, ceaser cipher, hill cipher, poly and mono alphabetic cipher.

UNIT - II

ENCRYPTION PRINCIPLES: Conventional encryption algorithms: Feistal structure, DES algorithm, S: Boxes, Triple DES, advanced data encryption standard (AES), cipher block modes of operation, location of encryption devices, Key distribution Approaches.

UNIT - III

CRYPTOGRAPHY AND APPLICATIONS : Public key cryptography principles, public key cryptography algorithms, digital signatures, RSA, elliptic algorithms, digital certificates, certificate authority and key management, Kerberos, X.509, directory authentication service. Message authentication, secure hash functions and HMAC.

UNIT - IV

ELECTRONIC MAIL SECURITY: Email privacy, PGP operations, radix: 64 conversions, key management for PGP, PGP trust model, multipurpose internet mail extension (MIME), secure/MIME(S/MIME).

UNIT - V

IP SECURITY ARCHITECTURE AND SERVICES: IP security overview, IP security architecture, security association, authentication header, encapsulating security payload, combining security associations and key management, OAKELY key determination protocol, ISAKMP.

UNIT - VI

WEB SECURITY: Web security considerations, secure socket layer (SSL) and transport layer security (TLS), secure electronic transaction (SET).

UNIT - VII

NETWORK MANAGEMENT SECURITY: Basic concepts of SNMP, SNMPv1 community facility and SNMPv3. System Security, intruders, intrusion techniques, intrusion detection, password management, bot nets.

UNIT - VIII

MALICIOUS SOFTWARE: Viruses and related threats, virus counter measures, distributed denial of service attacks.

FIREWALLS: Firewall design principles, trusted systems, common criteria for information technology security evolution.

TEXT BOOKS:

1. William Stallings (2007), *Network Security Essentials (Applications and Standards*), 3rd Edition, Pearson Education, New Delhi, India.
2. William Stallings (1998), *Cryptography and network Security*, 3rd Edition, Prentice Hall of India, New Delhi, India.

REFERENCE BOOKS:

1. Eric Maiwald (2004), *Fundamentals of Network Security*, Dreamtech press, India.
2. Charlie Kaufman, Radia Perlman, Mike Speciner (2002), *Network Security: Private Communication in a Public World*, 2nd Edition, Pearson Education, India.
3. Robert Bragg, Mark Rhodes (2004), *Network Security: The Complete Reference*, Tata Mcgraw Hill, New Delhi.
4. Buchmann (2004), *Introduction to Cryptography*, 2nd Edition, Springer, USA.

M. Tech. ES II SEMESTER

ROBOTICS AND AUTOMATION
(Professional Elective - IV)

Course Code: **B1616**

L	P	C
3	-	3

UNIT - I

INTRODUCTION TO ROBOTICS: History of Robots, Classifications, Various Fields of Robotics, Actuators, Sensors, Manipulators, End Effectors, Application Areas, Robot Programming Languages.

UNIT - II

BASIC CONCEPTS: Definition and Origin of Robotics, Different Types of Robotics, Various Generations of Robots, Degrees of Freedom, Asimov's Laws of Robotics, Dynamic Stabilization of Robots.

UNIT - III

MANIPULATORS, ACTUATORS AND GRIPPERS: Construction of Manipulators, Manipulator Dynamics and Force Control, Electronic and Pneumatic Manipulator Control Circuits, End Effectors, Various Types of Grippers, Design Considerations.

UNIT - IV

ROBOT KINEMATICS: Matrix Representation, Homogeneous Transformation, DH Representation of Standard Robots, Inverse Kinematics.

UNIT - V

ROBOT DYNAMICS: Velocity Kinematics, Jacobian and Inverse Jacobian, Lagrangian Formulation, Euler's Lagrangian Formulation, Robot Equation of Motion.

UNIT - VI

TRAJECTORY PLANNING: Introduction, Path Vs Trajectory, Joint-Space Vs Cartesian, Space Descriptions, Basics of Trajectory Planning, Joint-Space Trajectory Planning, Cartesian-Space Trajectories.

UNIT - VII

CONTROL AND APPLICATION OF ROBOTICS: Linear Control of Robot Manipulation, Second-Order Systems, Trajectory Following Control, Modeling and Control of Single Joint, Architecture of Industrial Robotic Controllers, Robot Applications.

UNIT - VIII

CASE STUDIES: Multiple Robots, Machine Interface, Robots in Manufacturing and Non- Manufacturing Applications, Robot Cell Design, Selection of Robot.

TEXTBOOKS:

1. Saced B. Niku (2001), *Introduction to Robotics Analysis, Systems, Applications*, Prentice Hall of India / Pearson Education, New Delhi, India.
2. Craig (2004), *Introduction to Robotics Mechanics and Control*, 2nd edition, Pearson Education, USA.

REFERENCE BOOKS:

1. Mikell P. Weiss G. M, Nagel R .N, Odraj N. G(1996), *Industrial Robotics*, McGraw-Hill, New Delhi, India.
2. Ghosh (1998), *Control in Robotics and Automation: Sensor Based Integration*, Allied Publishers, New Delhi.
3. K. S. Fu & Co (1991*), Robotics Control, Sensing, Vision and Intelligence,* McGraw Hill International*,* USA.
4. R. D. Klafter, T. A. Chimielewski, M. Negin (1994), *Robotic Engineering – An integrated Approach*, Prentice Hall of India, New Delhi, India.
5. Mikell P. Groover, Mitchell Weiss, Roger N. Nagel, Nicholas G. Odrey (2008), *Industrial Robotics Technology,* Tata McGraw-Hill, New Delhi, India.

M. Tech. ES II SEMESTER

APPLICATION OF MEMS
(Professional Elective - IV)

Course Code: **B1617**

L	P	C
3	-	3

UNIT - I

MICRO-FABRICATION: Overview of micro fabrication, essential overview of frequently used microabrication processes, the microelectronics fabrication process flow, silicon based mems processes, packaging and integration, new materials and fabrication processes, process selection and design concepts: conductivity of semiconductors-crystal planes and orientation-stress and strain-flexural beam analysis.

UNIT - II

MATERIALS AND ELECTROMECHANICAL CONCEPTS: Conductivity of semiconductors, crystal planes and orientations, stress and strain, flexural beam bending analysis under simple loading conditions, torsional deflections, intrinsic stress, dynamic system, resonant frequency and quality factor.

UNIT - III

ELECTROSTATIC SENSORS AND ACTUATORS: Introduction to electrostatic sensors and actuators, parallel plate capacitor, applications of parallel plate capacitor, interdigitated finger capacitors.

UNIT - IV

THERMAL SENSING AND ACTUATION: Introduction, sensors and actuators based on thermal expansion, thermo couples, thermal resistors, applications.

UNIT - V

PIEZO ELECTRIC MATERIALS, SENSING AND ACTUATION: Origin and expression piezoresistivity**,** piezoresistive sensor materials, stress analysis of mechanical elements, applications of piezoresistive sensors, properties of piezoelectric materials, applications.

UNIT - VI

MAGNETIC ACTUATION: Preview, essential concepts and principles, fabrication of micro-magnetic components, case studies of MEMS magnetic actuators.

UNIT - VII

POLYMERS MEMS: Introduction, Polymers in MEMS: Polyimide, SU-8, Liquid Crystal Polymer (LCP) ,PDMS ,PMMA, Parylene, Fluorocarbon, Representative Applications.

UNIT - VIII

CASE STUDIES: Case Studies Of Selected MEMS Products**:** Blood Pressure Sensors, Microphone, Acceleration Sensors, Gyros.

TEXTBOOKS:

1. Chang Liu (2010), *Foundations of MEMS*, 2nd edition, Pearson International Edition, New Jersy, USA.
2. Marc Madou (1997), *Fundamentals of Micro fabrication*, CRC Press, USA.

REFERENCE BOOKS:

1. M. H. Bao (2000), *Micromechanical Transducers: Pressure sensors, accelerometers and gyroscopes*, Elsevier, China.
2. W. Trimmer (1996), *Micromechanics and MEMS: Classic and Seminal Papers*, IEEE Press, New Jersy, USA.

M. Tech. ES II SEMESTER

EMBEDDED SYSTEM LAB USING PSOC

Course Code: **B1618**

L	P	C
-	3	2

LIST OF EXPERIMENTS:

1. Interface Seven Segment Display with 8051 Microcontroller.
2. Interface LEDs with 8051 Microcontroller.
3. Develop a program to perform Encryption and Decryption
4. Interface LCD with 8051 Microcontroller
5. Develop a program to read data from Sensor and to display data.
6. Serial Communication between Microcontrollers to PC vice versa
7. Interfacing Switches with 8051 Microcontroller.
8. Interface ADC with 8051 Microcontroller.
9. Port RTOS (µCos) to 8051 Board.
10. Simulate on elevator movement using RTOS on 8051 board.
11. Simulate coffee vending machine
12. Simulating Flash memory using PSOC.
13. Understanding serial communication between PC to PCin PSOC.
14. Designing of any automated system using PSOC.

Note: All the following experiments are expected to run by using PSOC

M. Tech. ES I / II SEMESTER

TECHNICAL SEMINAR

L	T	P	C
-	-	-	2

1. OBJECTIVE:

Seminar is an important component of learning in an Engineering College, where the student gets acquainted with preparing a report & presentation on a topic.

2. **PERIODICITY / FREQUENCY OF EVALUATION: Twice**

3. PARAMETERS OF EVALUATION:

1. The seminar shall have two components, one chosen by the student from the course-work without repetition and approved by the faculty supervisor. The other component is suggested by the supervisor and can be a reproduction of the concept in any standard research paper or an extension of concept from earlier course work.
2. The two components of the seminar are distributed between two halves of the semester and are evaluated for 50 marks each. The average of the two components shall be taken as the final score.
3. The students shall be required to submit the rough drafts of the seminar outputs within one week of the commencement of the class work.
4. Supervisor shall make suggestions for modification in the rough draft. The final draft shall be presented by the student within a week thereafter.
5. Presentation schedules will be prepared by different Departments in line with the academic calendar.

The Seminars shall be evaluated in two stages as follows:

A. Rough draft

In this stage, the student should collect information from various sources on the topic and collate them in a systematic manner. He/ She may take the help of the concerned supervisor.

The report should be typed in “MS-Word” file with “calibri” font, with font size of 16 for main heading, 14 for sub-headings and 11 for the body text. The contents should also be arranged in Power Point Presentation with relevant diagrams, pictures and illustrations. It should normally contain 18 to 25 slides, consisting of the followings:

1.	Topic, name of the student & guide	1 Slide
2.	List of contents	1 Slide
3.	Introduction	1 - 2 Slides
4.	Descriptions of the topic (point-wise)	7 - 10 Slides
5.	Images, circuits etc.	6 - 8 Slides
6.	Conclusion	1 - 2 Slides
7.	References/Bibliography	1 Slide

The soft copy of the rough draft of the seminar presentation in MS Power Point format along with the draft Report should be submitted to the concerned supervisor, with a copy to the concerned HOD within 30 days of the commencement of class work.

The evaluation of the Rough draft shall generally be based upon the following.

1.	Punctuality in submission of rough draft and discussion	2 Marks
2.	Resources from which the seminar have been based	2 Marks
3.	Report	3 Marks
4.	Lay out, and content of Presentation	3 Marks
5.	Depth of the students knowledge in the subject	5 Marks
Total		15 Marks

After evaluation of the first draft the supervisor shall suggest further reading, additional work and fine tuning, to improve the quality of the seminar work.

Within 7 days of the submission of the rough draft, the students are to submit the final draft incorporating the suggestions made by the supervisor.

B. Presentation:

After finalization of the final draft, the students shall be allotted dates for presentation (in the designated seminar classes) and they shall then present it in presence students, supervisor, faculties of the department and at least one faculty from some department / other department.

The student shall submit 3 copies of the Report neatly bound along with 2 soft copies of the PPT in DVD medium. The students shall also distribute the title and abstract of the seminar in hard copy to the audience. The final presentation has to be delivered with 18-25 slides.

The evaluation of the Presentation shall generally be based upon the following.

1.	Contents	10 Marks
2.	Delivery	10 Marks
3.	Relevance and interest the topic creates	5 Marks
4.	Ability to involve the spectators	5 Marks
5.	Question answer session	5 Marks
Total		35 Marks

4. WHO WILL EVALUATE?

The presentation of the seminar topics shall be made before an internal evaluation committee comprising the Head of the Department or his/her nominee, seminar supervisor and a senior faculty of the department / other department.

M. Tech. ES III SEMESTER

COMPREHENSIVE VIVA

Course Code: **B1620**

L	T	P	C
-	-	-	4

1. OBJECTIVE:

- To enable the examiners to assess the candidate's knowledge in his or her particular field of learning.
- To test the student's awareness of the latest developments and relate them to the knowledge acquired during the classroom teaching.

2. PARAMETERS OF EVALUATION:

Subject Knowledge	Current Awareness	Career Orientation	Communication Skills	Total
20	10	10	10	50

3. WHO WILL EVALUATE?

The comprehensive Viva will be conducted by a committee comprising Head of the Department or his/her nominee, two senior faculty of the respective department and an external examiner from outside the college. The comprehensive viva shall be evaluated for 50 marks at the end of III semester. A minimum of 40% of maximum marks shall be obtained to earn the corresponding credits.

4. **PERIODICITY / FREQUENCY OF EVALUATION: Once**

5. PEDAGOGY:

- The viva will be held on a face to face basis.
- The students will be expected to answer the questions related to latest developments and all courses taken till date.
- Viva voce will be conducted within week before the beginning of midterm examinations. However, in exceptional circumstances it can be scheduled immediately after the end of midterm examinations.
- Students will have to make themselves available on the date of the viva voce.

M. Tech. ES III/ IV SEMESTER

PROJECT WORK

1. OBJECTIVE:

The main objective of the Project Work is for the students to learn and experience all the major phases and processes involved in solving "real life engineering problems".

2. EXPECTED OUTCOME:

The major outcome of the M. Tech project must be well-trained students. More specifically students must have acquired:

- System integration skills
- Documentation skills
- Project management skills
- Problem solving skills

3. PROJECT SELECTION:

Projects are suggested by the faculty, with or without collaboration with an industry. All faculty are to suggest projects. Students are also encouraged to give project proposals after identifying a faculty who would be willing to supervisor the work. A Project brief is to be given by the faculty to the group defining the project comprehensively.

All M. Tech major projects are to be done in the Institute. For industry specified projects, students will be permitted to spend 1-2 weeks in the industry on recommendation by the supervisor. The number of students per batch should be 1.

4. WHO WILL EVALUATE?

The end semester examination shall be based on the report submitted and a viva-voce exam for 100 marks by committee comprising of the Head of the Department, project supervisor and an external examiner.

5. EVALUATION:

The basic purpose is to assess the student competencies with regard to his project work. More specifically to assess the student's individual contribution to the project, to establish the level of understanding of basic theoretical knowledge relevant to the project and to ensure that the student has good understanding and appreciation of design and development decisions taken in the course of the project. It is desirable that all faculty members are present for the evaluations as this is a platform to get to know the student projects and to motivate the students to do good projects. The faculty should adopt a clear and consistent pattern of asking questions from general to specific aspects of the project. The presentation and evaluation is open to other students of the department.

The project work shall be evaluated for 150 marks out of which 50 marks for internal evaluation and 100 marks for end-semester evaluation. The evaluation shall be done on the following basis

Semester III	**Semester IV**
Preliminary Evaluation - 50 marks	Design Evaluation I - 25 marks
	Design Evaluation II - 25 marks
	Final Evaluation – 100 marks

6. GUIDELINES FOR THE PREPARATION OF M. TECH PROJECT REPORTS

1.1. Project reports should be typed neatly only on one side of the paper with 1.5 or double line spacing on a A4 size bond paper (210 x 297 mm). The margins should be: Left - 1.25", Right - 1", Top and Bottom - 0.75".

1.2. The total number of reports to be prepared are:

- One copy to the department
- One copy to the concerned guide(s)
- One copy to the candidate.

1.3. Before taking the final printout, the approval of the concerned guide(s) is mandatory and suggested corrections, if any, must be incorporated.

1.4. For making copies dry tone Xerox is suggested.

1.5. Every copy of the report must contain

- Inner title page (White)
- Outer title page with a plastic cover
- Certificate in the format enclosed both from the college and the organization where the project is carried out.
- An abstract (synopsis) not exceeding 100 words, indicating salient features of the work.

6.6. The organization of the report should be as follows:

1.	Inner title page	Usually numbered in roman
2.	Abstract or Synopsis	
3.	Acknowledgments	
4.	Table of Contents	
5.	List of table & figures (optional)	

6.7 Chapters (to be numbered) containing Introduction, which usually specifies the scope of work and its importance and relation to previous work and the present developments, Main body of the report divided appropriately into chapters, sections and subsections.

- The chapters, sections and subsections may be numbered in the decimal form for e.g. Chapter 2, sections as 2.1, 2.2 etc., and subsections as 2.2.3, 2.5.1 etc.
- The report should be typed in "MS-Word" file with "calibri" font. The chapter must be left or right justified (font size 16). Followed by the title of chapter centered (font size 18), section/subsection numbers along with their headings must be left justified with section number and its heading in font size 16 and subsection and its heading in font size 14. The body or the text of the report should have font size 11.
- The figures and tables must be numbered chapter wise for e.g.: Fig. 2.1 Block diagram of a serial binary adder, Table 3.1 Primitive flow table, etc.
- The last chapter should contain the summary of the work carried, contributions if any, their utility along with the scope for further work.

6.8. Reference OR Bibliography: The references should be **numbered serially** in the order of their occurrence in the text and their numbers should be indicated within square brackets for e.g. [3]. The section on references should list them in serial order in the following format.

1. For textbooks - A.V. Oppenheim and R.W. Schafer, Digital Signal Processing, Englewood, N.J., Prentice Hall, 3 Edition, 1975.
2. For papers - Devid, Insulation design to combat pollution problem, Proc of IEEE, PAS, Vol 71, Aug 1981, pp 1901-1907.

6.9. Only SI units are to be used in the report. Important equations must be numbered in decimal form for e.g. **V = IZ** ..... **(3.2)**

6.10. All equation numbers should be right justified.

6.11. The project report should be brief and include descriptions of work carried out by others only to the minimum extent necessary. Verbatim reproduction of material available elsewhere should be strictly avoided. Where short excerpts from published work are desired to be included, they should be within quotation marks appropriately referenced.

6.12. Proper attention is to be paid not only to the technical contents but also to the organization of the report and clarity of the expression. Due care should be taken to avoid spelling and typing errors. The student should note that report-write-up forms the important component in the overall evaluation of the project

6.13. Hardware projects must include: the component layout, complete circuit with the component list containing the name of the component, numbers used, etc. and the main component data sheets as Appendix. At the time of report submissions, the students must hand over a copy of these details to the project coordinator and see that they are entered in proper registers maintained in the department.

6.14. Software projects must include a virus free disc, containing the software developed by them along with the read me file. Read me file should contain the details of the variables used, salient features of the software and procedure of using them: compiling procedure, details of the computer hardware/software requirements to run the same, etc. If the developed software uses any public domain software downloaded from some site, then the address of the site along with the module name etc. must be included on a separate sheet. It must be properly acknowledged in the acknowledgments.

6.15. Sponsored Projects must also satisfy the above requirements along with statement of accounts, bills for the same dully attested by the concerned guides to process further, They must also produce NOC from the concerned guide before taking the internal viva examination.

6.16. The reports submitted to the department/guide(s) must be hard bounded, with a plastic covering.

6.17. Separator sheets, used if any, between chapters, should be of thin paper

VARDHAMAN COLLEGE OF ENGINEERING

(Autonomous)

Shamshabad – 501 218, Hyderabad

Department of ……..

CERTIFICATE

Certified that the project work entitled …….. carried out by Mr./Ms. ……..., Roll Number ……, a bonafide student of ……in partial fulfillment for the award of **Master of Technology** in …… of the Jawaharlal Nehru Technological University, Hyderabad during the year …….. It is certified that all corrections / suggestions indicated for Internal Assessment have been incorporated in the Report deposited in the departmental library. The project report has been approved as it satisfies the academic requirements in respect of Project work prescribed for the said Degree.

Name & Signature of the Guide **Name Signature of the HOD** **Signature of the Principal**

External Viva

Name of the examiners Signature with date

1.

2.

Certificate issued at the Organization where the project was carried out

(On a separate sheet, If applicable)

NAME OF THE INDUSTRY / ORGANIZATION, Address with pin code

CERTIFICATE

Certified that the project work entitled …….. carried out by Mr./Ms . ……., Roll Number……., a bonafide student of ……in partial fulfillment for the award of **Master of Technology** in …… of the Jawaharlal Nehru Technological University, Hyderabad during the year …….. It is certified that, he/she has completed the project satisfactorily

Name & Signature of the Guide **Name & Signature of the Head of Organization**

7. **DISTRIBUTION OF MARKS FOR M.TECH DISSERTATION EVALUATION**

S No.	Particulars	Max. Marks
1	Relevance of the subject in the present context	**10**
2	Literature Survey	**10**
3	Problem formulation	**10**
4	Experimental observation / theoretical modeling	**10**
5	Results – Presentation & Discussion	**20**
6	Conclusions and scope for future work	**10**
7	Overall presentation of the Thesis / Oral presentation	**20**
8	Project Report Writing	**10**
Total Marks		**100**

MALPRACTICES RULES
DISCIPLINARY ACTION FOR / IMPROPER CONDUCT IN EXAMINATIONS

	Nature of Malpractices/Improper conduct	Punishment
	If the candidate:	
1. (a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination)	Expulsion from the examination hall and cancellation of the performance in that subject only.
(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2.	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that Semester/year. The Hall Ticket of the candidate is to be cancelled and sent to the University.
3.	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred and forfeits the seat. The performance of the original candidate, who has been impersonated, shall be cancelled in all the subjects of the examination (including practicals and project work) already appeared and shall not be allowed to appear for examinations of the remaining subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.
4.	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5.	Uses objectionable, abusive or offensive language in	Cancellation of the performance in that subject.

	the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	
6.	Refuses to obey the orders of the Chief Superintendent/Assistant – Superintendent / any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in charge or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer-in-charge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The candidates also are debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case is registered against them.
7.	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
8.	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat.
9.	If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	Student of the colleges expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the College will be handed over to police and, a police case will be registered against them.
10.	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject

		and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year.
11.	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester/year examinations.
12.	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the University for further action to award suitable punishment.	

Frequently asked Questions and Answers about autonomy

1. Who grants Autonomy? UGC, Govt., AICTE or University

In case of Colleges affiliated to a university and where statutes for grant of autonomy are ready, it is the respective University that finally grants autonomy.

2. Shall VCE award its own Degrees?

No. Degree will be awarded by Jawaharlal Nehru Technological University, Hyderabad with a mention of the name Vardhaman College of Engineering on the Degree Certificate.

3. What is the difference between a Deemed University and an Autonomy College?

A Deemed University is fully autonomous to the extent of awarding its own Degree. A Deemed University is usually a Non-Affiliating version of a University and has similar responsibilities like any University. An Autonomous College enjoys Academic Autonomy alone. The University to which an autonomous college is affiliated will have checks on the performance of the autonomous college.

4. How will the Foreign Universities or other stake – holders know that we are an Autonomous College?

Autonomous status, once declared, shall be accepted by all the stake holders. Foreign Universities and Indian Industries will know our status through our college website.

5. What is the change of Status for Students and Teachers if we become Autonomous?

An autonomous college carries a prestigious image. Autonomy is actually earned out of continued past efforts on academic performances, capability of self-governance and the kind of quality education we offer.

6. Who will check whether the academic standard is maintained / improved after Autonomy? How will it be checked?

There is a built in mechanism in the autonomous working for this purpose. An Internal Committee called Academic Programme Evaluation Committee is a Non – Statutory body, which will keep a watch on the academics and keep its reports and recommendations every year. In addition to Academic Council, the highest academic body also supervises the academic matters. At the end of three years, there is an external inspection by the University for this purpose. The standards of our question papers, the regularity of academic calendar, attendance of students, speed and transparency of result declaration and such other parameters are involved in this process.

7. Will the students of VCE as an Autonomous College qualify for University Medals and Prizes for academic excellence?

No. VCE has instituted its own awards, medals, etc. for the academic performance of the students. However for all other events like sports, cultural and co-curricular organized by the University the students shall qualify.

8. Can VCE have its own Convocation?

No, since the University awards the Degree the Convocation will be that of the University.

9. Can VCE give a provisional degree certificate?

Since the examinations are conducted by VCE and the results are also declared by VCE, the college sends a list of successful candidates with their final percentage of marks to the University. Therefore with the prior permission of the University the college will be entitled to give the provisional certificate.

10. Will Academic Autonomy make a positive impact on the Placements or Employability?

Certainly. The number of students qualifying for placement interviews is expected to improve, due to rigorous and repetitive classroom teaching and continuous assessment, besides the autonomous status is more responsive to the needs of the industry. As a result, there will be a lot of scope for industry oriented skill development built-in into the system. The graduates from an autonomous college will therefore represent better employability.

11. What is the proportion of Internal and External Assessment as an Autonomous College?

Presently, it is 25 % for internal assessment and 75 % for external assessment. As the autonomy matures the internal assessment component shall be increased at the cost of external assessment.

12. Will there be any Revaluation or Re-Examination System?

No. There will not be any Revaluation system or Re-examination. But, there is a personal verification of the answer scripts.

13. How fast Syllabi can be and should be changed?

Autonomy allows us the freedom to change the syllabi as often as we need.

14. Will the Degree be awarded on the basis of only final year performance?

No. The percentage of marks will reflect the average performance of all the semesters put together.

15. Who takes Decisions on Academic matters?

The Academic Council of College is the top academic body and is responsible for all the academic decisions. Many decisions are also taken at the lower level like the BOS which are like Boards of Studies of the University.

16. What is the role of Examination committee?

The Exam Committee is responsible for the smooth conduct of inter and external examinations. All matters involving the conduct of examinations, spot valuations, tabulations, preparation of Memorandum of Marks etc fall within the duties of the Examination Committee.

17. Is there any mechanism for Grievance Redressal?

Yes, the college has grievance redressal committee, headed by a senior faculty member of the college.

18. How many attempts are permitted for obtaining a Degree?

All such matters are defined in Rules & Regulations.

19. Who declares the result?

The result declaration process is also defined. After tabulation work the entire result is reviewed by the Moderation Committee. Any unusual deviations or gross level discrepancies are deliberated and removed. The entire result is discussed in the College Academic Council for its approval. The result is then declared on the college notice boards as well put on the web site of the college. It is eventually sent to the University.

20. What is our relationship with the Jawaharlal Nehru Technological University, Hyderabad?

We remain an affiliated college of the Jawaharlal Nehru Technological University, Hyderabad. The University has the right to nominate its members on the academic bodies of the college.

21. Shall we require University approval if we want to start any New Courses?
Yes, It is expected that approvals or such other matters from an autonomous college will receive priority.

22. Shall we get autonomy for PG and Doctoral Programmes also?
Yes, presently our PG programmes are also enjoying autonomous status.

23. How many exams will be there as an autonomous college?
This is defined in the Rules & Regulations.