VARDHAMAN COLLEGE OF ENGINEERING

(AUTONOMOUS)

(Permanently Affiliated to JNTUH, Approved by AICTE, New Delhi and Accredited by NBA)

Shamshabad – 501 218, Hyderabad

MASTER OF TECHNOLOGY
DIGITAL ELECTRONICS AND COMMUNICATION SYSTEMS

ACADEMIC REGULATIONS, COURSE STRUCTURE AND SYLLABI FOR M.TECH – DIGITAL ELECTRONICS AND COMMUNICATION SYSTEMS UNDER AUTONOMOUS STATUS FOR THE BATCHES ADMITTED FROM THE ACADEMIC YEAR 2011 - 12

Note: The regulations hereunder are subject to amendments as may be made by the Academic Council of the College from time to time. Any or all such amendments will be effective from such date and to such batches of candidates (including those already undergoing the program) as may be decided by the Academic Council.

PRELIMINARY DEFINITIONS AND NOMENCLATURES

- "Autonomous Institute / College" means an institute / college designated as autonomous institute / college by the Jawaharlal Nehru Technological University, Hyderabad (JNTUH), as per the JNTUH Autonomous College Statutes, 2011.

- "Academic Autonomy" means freedom to a College in all aspects of conducting its academic programs, granted by the University for promoting excellence.

- "Commission" means University Grants Commission.

- "AICTE" means All India Council for Technical Education.

- "University" the Jawaharlal Nehru Technological University, Hyderabad.

- "College" means Vardhaman College of Engineering, Hyderabad unless indicated otherwise by the context.

- "Program" means:
  Bachelor of Technology (B.Tech) degree program
  UG Degree Program: B.Tech
  PG degree Program: M.Tech

- "Branch" means specialization in a program like M.Tech degree program in Power Electronics and Electrical Drives.

- "Course" or "Subject" means a theory or practical subject, identified by its course – number and course-title, which is normally studied in a semester. For example, ABS11T01: Mathematics - I, ACS11T02: Data Structures through C, etc.

- T – Tutorial, P – Practical, D – Drawing, L - Theory, C - Credits

FOREWORD

The autonomy is conferred on Vardhaman College of Engineering by J N T University, Hyderabad based on its performance as well as future commitment and competency to impart quality education. It is a mark of its ability to function independently in accordance with the set norms of the monitoring bodies like UGC and AICTE. It reflects the confidence of the affiliating University in the autonomous institution to uphold and maintain standards it expects to deliver on its own behalf and thus awards degrees on behalf of the college. Thus, an autonomous institution is given the freedom to have its own **curriculum, examination system** and **monitoring mechanism**, independent of the affiliating University but under its observance.

Vardhaman College of Engineering is proud to win the credence of all the above bodies monitoring the quality in education and has gladly accepted the responsibility of sustaining, if not improving upon the standards and ethics for which it has been striving for more than a decade in reaching its present standing in the arena of contemporary technical education. As a follow up, statutory bodies like Academic Council and Boards of Studies are constituted with the guidance of the Governing Body of the College and recommendations of the JNTU Hyderabad to frame the regulations, course structure and syllabi under autonomous status.

The autonomous regulations, course structure and syllabi have been prepared after prolonged and detailed interaction with several expertise solicited from academics, industry and research, in accordance with the vision and mission of the college to order to produce a quality engineering graduate to the society.

All the faculty, parents and students are requested to go through all the rules and regulations carefully. Any clarifications needed are to be sought at appropriate time and with principal of the college, without presumptions, to avoid unwanted subsequent inconveniences and embarrassments. The Cooperation of all the stake holders is sought for the successful implementation of the autonomous system in the larger interests of the college and brighter prospects of engineering graduates.

PRINCIPAL

VARDHAMAN COLLEGE OF ENGINEERING

(Autonomous)

(Permanent Affiliation with JNTUH, Approved by AICTE, New Delhi and Accredited by NBA)

ACADEMIC REGULATIONS

M.Tech. Regular Two Year Post-Graduate Programme

(For the batches admitted from the academic year 2011–12)

For pursuing Two year degree program of study in Master of Technology (M.Tech.) offered by Vardhaman College of Engineering under Autonomous status and herein after referred to as VCE:

1. APPLICABILITY

All the rules specified herein, approved by the Academic Council, will be in force and applicable to students admitted from the academic year 2011-2012 onwards. Any reference to "College" in these rules and regulations stands for Vardhaman College of Engineering.

2. EXTENT

All the rules and regulations, specified herein after shall be read as a whole for the purpose of interpretation and as and when a doubt arises, the interpretation of the Chairman, Academic Council is final. As per the requirements of statutory bodies Principal, Vardhaman College of Engineering shall be the Chairman, Academic Council.

3. PROGRAMS OFFERED

Vardhaman College of Engineering, an autonomous college affiliated to JNTUH, offers the following M.Tech programmes of study leading to the award of M.Tech degree under the autonomous scheme.

S. No	M.Tech Courses	Intake
1	Computer Science and Engineering	36
2	Software Engineering	18
3	Digital Electronics and Communication Systems	36
4	Wireless and Mobile Communications	18
5	Power Electronics and Electrical Drives	18

4. ADMISSION

Admission into first year of Two Year M.Tech Program shall be made subject to the eligibility, qualifications and specialization as per the guidelines prescribed by the APSCHE and AICTE from time to time.

5. DURATION OF THE PROGRAMS

5.1 Normal Duration

M.Tech degree program extends over a period of two academic years leading to the Degree of Master of Technology (M.Tech) of the Jawaharlal Nehru Technology University, Hyderabad.

5.2 Maximum Duration

5.2.1 The maximum period within which a student must complete a full-time academic program is 4 years for M.Tech. If a student fails to complete the academic program within the maximum duration as specified above, he / she will be required to withdraw from the program.

5.2.3 The period is reckoned from the academic year in which the student is admitted first time into the degree programme.

6. SEMESTER STRUCTURE

The College shall follow semester pattern. An academic year shall consist of a first semester and a second semester and the summer term. Each semester shall be of 23 weeks duration and this period includes time for course work, examination preparation, and conduct of examinations. Each semester shall have a minimum of 90 working days. The academic calendar is shown in Table 1 is declared at the start of the semester. The duration for each semester shall be a minimum of 17 weeks of instruction.

Table 1: Academic Calendar

FIRST SEMESTER (23 weeks)	I Spell Instruction Period	: 9 weeks	19 weeks
	I Mid Examinations	: 1 week	
	II Spell Instruction Period	: 8 weeks	
	II Mid Examinations	: 1 Week	
	Preparation & Practical Examinations		2 weeks
	External Examinations		2 weeks
Semester Break			2 weeks
SECOND SEMESTER (23 weeks)	I Spell Instruction Period	: 9 weeks	19 weeks
	I Mid Examinations	: 1 week	
	II Spell Instruction Period	: 8 weeks	
	II Mid Examinations	: 1 Week	
	Preparation & Practical Examinations		2 weeks
	External Examinations		2 weeks
Summer Vacation			4 weeks
THIRD SEMESTER	Project Work Phase – I		18 Weeks
FOURTH SEMESTER	Project Work Phase – II		18 Weeks

7. CREDIT BASED SYSTEM

All the academic programs under autonomy are based on credit system. Credits are assigned based on the following norms:

7.1. The duration of each semester will normally be 23 weeks with 5 days a week. A working day shall have 6 periods each of 60 minutes duration.

- 1 credit per lecture period per week
- 2 credits for three (or more) period hours of practicals
- 2 credits for technical seminar
- 4 credits for comprehensive viva examination
- 18 credits for project work phase – I
- 22 credits for project work phase – II

7.2. The two year curriculum of any M.Tech programme of study shall have total of 88 credits. The exact requirements of credits for each course will be as recommended by the Board of Studies concerned and approved by the Academic Council.

7.3. For courses like technical seminar / comprehensive viva / Project Work Phases – I and II, where formal contact hours are not specified, credits are assigned based on the complexity of the work to be carried out.

8. METHOD OF EVALUATION

The performance of a student in each semester shall be evaluated subject-wise with a maximum of 100 marks each for theory and 100 marks for practical, on the basis of Internal Evaluation and End Semester Examination.

8.1 Theory

For all lecture based theory courses, the evaluation shall be for 40 marks through internal evaluation and 60 marks through external end semester examination of three hours duration.

8.1.1. Internal evaluation

For theory subjects, during the semester there shall be 2 midterm examinations. Each midterm examination consists of subjective test. The subjective test is for 40 marks, with duration of 2 hours. The Mid-Term Examination question paper shall be set with **six** questions out of which **four** are to be answered. All questions carry equal marks.

First midterm examination shall be conducted for I – IV units of syllabus and second midterm examination shall be conducted for the remaining portion.

The internal marks shall be computed as the average of the two internal evaluations, of two subjective tests.

8.1.2. External Evaluation

The question paper shall be set externally and valued both internally and externally. The external end semester examination question paper in theory subjects will be for a maximum of 60 marks to be answered in three hours duration. For End-Semester examination, the candidate has to answer any five out of eight questions. Each question carries 12 marks. Each theory course shall consist of eight units of syllabus.

8.2. Practicals

Practicals shall be evaluated for 100 marks, out of which 60 marks are for external examination and 40 marks are for internal evaluation. The 40 internal marks are distributed as 25 marks for day-to-day work and 15 marks for internal examination. The external end - examination shall be conducted by the teacher concerned and an external examiner from outside the college.

8.3. Technical Seminar

The seminar shall have two components, one chosen by the student from the course-work without repetition and approved by the faculty supervisor. The other component is suggested by the supervisor and can be a reproduction of the concept in any standard research paper or an extension of concept from earlier course work. A hard copy of the information on seminar topic in the form of a report is to be submitted for evaluation along with presentation. The presentation of the seminar topics shall be made before an internal evaluation committee comprising the Head of the Department or his/her nominee, seminar supervisor and a senior faculty of the department. The two components of the seminar are distributed between two halves of the semester and are evaluated for 50 marks each. The average of the two components shall be taken as the final score. A minimum of 50% of maximum marks shall be obtained to earn the corresponding credits.

8.4. **Comprehensive Viva**

The comprehensive Viva will be conducted by a committee comprising Head of the Department or his/her nominee, two senior faculty of the respective department and an external examiner from outside the college. This is aimed at assessing the student's understanding of various subjects studied during the entire program. The comprehensive viva shall be evaluated for 50 marks at the end of III semester. A minimum of 50% of maximum marks shall be obtained to earn the corresponding credits.

8.5. **Project Work**

The project work shall be evaluated for 200 marks out of which 50 marks for phase – I internal evaluation, 50 marks for phase – II internal evaluation and 100 marks for end semester evaluation. A minimum of 50% of marks on the aggregate in the internal evaluation and external end-evaluation taken together shall be obtained to earn the corresponding credits.

Every candidate is required to submit dissertation after taking up a topic approved by the Departmental Committee. The project work shall be spread over in III semester and in IV semester. The project work shall be somewhat innovative in nature, exploring the research bent of mind of the student.

The Departmental Committee (DC) consists of HOD, Supervisor and two senior experts in the department. The committee monitors the progress of Project Work. The DC is constituted by the Principal on the recommendations of the department Head.

Student shall register for the Project work with the approval of Departmental Committee in the III Semester and continue the work in the IV Semester too. The Departmental Committee (DC) shall monitor the progress of the project work. In III Semester, Phase – I of the Project Work is to be completed. A Student has to identify the topic of work, collect relevant Literature, preliminary data, implementation tools / methodologies etc., and perform a critical study and analysis of the problem identified. He shall submit status report in two different phases in addition to oral presentation before the Departmental Committee for evaluation and award of 50 internal marks at the end of Phase – I.

A candidate shall continue the Project Work in IV Semester (Phase – II) and submit a Project report at the end of Phase – II after approval of the Departmental Committee. During Phase – II, the student shall submit status report in two different phases, in addition to oral presentation before the DC. The DC shall evaluate the project for 50 internal marks based on the progress, presentations and quality of work.

A candidate shall be allowed to submit the dissertation only after passing all the courses of I and II semesters with the approval of Departmental Committee not earlier than **40 weeks** from the date of registration of the project work and then take viva-voce examination. The viva-voce examination may be conducted once in three months for all the eligible candidates.

Three copies of the dissertation certified in the prescribed form by the supervisor and HOD shall be presented to the Department and one copy is to be submitted to the Controller of Examinations, VCE and one copy to be sent to the examiner.

The department shall submit a panel of three experts for a maximum of 5 students at a time. However, the examiners for conducting viva-voce examination shall be nominated by the Controller of Examinations, VCE. If the report of the examiner is favorable, viva-voce examination shall be conducted by a board consisting of the Supervisor, Head of the Department and the examiner who adjudicated the dissertation. The board shall jointly evaluate the project work for 100 marks. The candidates who fail in viva-voce examinations shall have to re-appear the viva-voce examination after three months. If he fails again in the second viva-voce examination, the candidate has to re-register for the Project Work.

If a candidate desires to change the topic of the project already chosen during Phase – I, he has to re-register for Project work with the approval of the DC and repeat Phases – I and II. Marks already earned in Phase – I stand cancelled.

9. ATTENDANCE REQUIREMENTS TO APPEAR FOR THE SEMESTER-END EXAMINATION

9.1. A student shall be eligible to appear for semester-end examinations if he acquires a minimum of 75% of attendance in aggregate of all the subjects in a semester.

9.2. Condonation of shortage of attendance in aggregate upto 10% (65% and above and below 75%) in each semester may be granted by the College Academic Committee.

9.3. Shortage of attendance below 65% in aggregate shall in no case be condoned.

9.4. Students whose shortage of attendance is not condoned in any semester are not eligible to take their semester-end examination of that class and their registration shall stand cancelled.

9.5. A student will not be promoted to the next semester unless he satisfies the attendance requirements of the current semester. The student may seek readmission for the semester when offered next. He will not be allowed to register for the subjects of the semester while he is in detention. A student detained due to shortage of attendance, will have to repeat that semester when offered next.

9.6. A stipulated fee shall be payable towards condonation of shortage of attendance to the College.

9.7. Attendance may also be condoned as per the recommendations of academic council for those who participate in prestigious sports, co-curricular and extra-curricular activities provided as per the Govt. of AP norms in vogue.

10. ACADEMIC REQUIREMENTS FOR PROMOTION / COMPLETION OF REGULAR M.TECH PROGRAMME OF STUDY

The following academic requirements have to be satisfied in addition to the attendance requirements for promotion / completion of regular M.Tech programme of study.

i. A student shall be deemed to have satisfied the minimum academic requirements for each theory, and practical, if he secures not less than 40% of marks in the semester-end examination and a minimum of 50% of marks in the sum of the internal evaluation and semester - end examination taken together.

ii. In case of technical seminar and comprehensive viva a student shall be deemed to have satisfied the minimum academic requirements and earned the credits allotted to each of them if he/she secures not less than 50% of marks.

iii. In case of project work, a student shall be deemed to have satisfied the minimum academic requirements and earned the credits allotted if he/she secures not less than 50% of marks on the aggregate in the internal evaluation and external end-evaluation taken together.

iv. A student shall register for all the 88 credits and earn all the 88 credits. Marks obtained in all the 88 credits shall be considered for the award of the class based on aggregate of marks.

v. A student who fails to earn 88 credits as indicated in the course structure within **FOUR** academic years from the year of their admission shall forfeit their seat in M.Tech programme and their admission stands cancelled.

viii. Students who are detained for want of attendance (or) who have not fulfilled academic requirements (or) who have failed after having undergone the course in earlier regulations (or) have discontinued and wish to continue the course are eligible for admission into the unfinished semester from the date of commencement of class work with the same (or) equivalent subjects as and when subjects are offered, and pursue the remaining course work with the academic regulations of the batch into which such students are readmitted. However, all such readmitted students shall earn all the credits of subjects they have pursued for completion of the course.

11. EVALUATION

Following procedure governs the evaluation.

11.1. Marks for components evaluated internally by the faculty should be submitted to the Controller of Examinations one week before the commencement of the semester-end examinations. The marks for the internal evaluation components will be added to the external evaluation marks secured in the semester-end examinations, to arrive at total marks for any subject in that semester.

11.2. Performance in all the courses is tabulated course-wise and will be scrutinized by the Examination Committee and moderation is applied if needed, based on the recommendations of moderation committee and course-wise marks lists are finalized.

11.3. Student-wise tabulation is done and student-wise memorandum of marks is generated which is issued to the student.

12. SUPPLEMENTARY EXAMINATION

Supplementary examinations for the odd semester shall be conducted with the regular examinations of even semester and vice versa, for those who appeared and failed in regular examinations. Such of the candidates writing supplementary examinations may have to write more than one examination per day.

13. RE-REGISTRATION FOR IMPROVEMENT OF INTERNAL

Following are the conditions to avail the benefit of improvement of internal marks.

13.1. The candidate should have completed the course work and obtained examinations results for I & II semesters.

13.2. A candidate shall be given one chance for a maximum of Three Theory subjects for Improvement of Internal evaluation marks for which the candidate has to re-register for the chosen subjects and fulfill the academic requirements.

13.3. For each subject, the candidate has to pay a fee equivalent to one third of the semester tuition fee and the amount is to be remitted in the form of D.D. in favour of the Principal, Vardhaman College of Engineering payable at Hyderabad along with the requisition through the concerned Head of the Department.

13.4. In the event of availing the Improvement of Internal evaluation marks, the internal evaluation marks as well as the End Examinations marks secured in the previous attempt(s) for the re-registered subjects stand cancelled.

14. PERSONAL VERIFICATION

Students shall be permitted for personal verification of the semester-end examination answer scripts within a stipulated period after payment of prescribed fee.

15. TRANSITORY REGULATIONS

Students who are detained for want of attendance (or) who have not fulfilled academic requirements (or) who have failed after having undergone the course in earlier regulations (or) have discontinued and wish to continue the course are eligible for admission into the unfinished semester from the date of commencement of class work with the same (or) equivalent subjects as and when subjects are offered, and pursue the remaining course work with the academic regulations of the batch into which such students are readmitted. A regular student has to satisfy all the eligibility requirements within the maximum stipulated period of four years for the award of M.Tech Degree.

16. TRANSCRIPTS

After successful completion of the entire programme of study, a transcript containing performance of all academic years will be issued as a final record. Transcripts will also be issued, if required, after payment of requisite fee. Partial transcript will also be issued upto any point of study to a student on request, after payment of requisite fee.

17. AWARD OF DEGREE

The degree will be conferred and awarded by Jawaharlal Nehru Technological University, Hyderabad on the recommendations of the Chairman, Academic Council.

17.1. Eligibility

A student shall be eligible for the award of M.Tech. Degree, if he fulfills all the following conditions:

i. Registered and successfully completed all the components prescribed in the programme of study to which he is admitted.

ii. Successfully acquired the minimum required credits as specified in the curriculum corresponding to the branch of study within the stipulated time.

iii. Obtained not less than 50% of marks (minimum requirement for declaring as passed).

iv. Has no dues to the college, hostel, and library etc. and to any other amenities provided by the College.

v. No disciplinary action is pending against him.

17.2. Award of Class

Declaration of Class is based on percentage of marks to be secured.

After a student has satisfied the requirement prescribed for the completion of the programme and is eligible for the award of M.Tech. Degree he shall be placed in one of the following four classes Shown in Table 4:

Table 4: Declaration of Class is based on percentage of marks to be secured

Class Awarded	% of marks to be secured	
First Class with Distinction	70% and above	From the aggregate marks secured for the 88 Credits.
First Class	Below 70% but not less than 60%	
Second Class	Below 60% but not less than 50%	
Fail	Below 50%	

Sometimes, it is necessary to provide equivalence of percentages and/or *Class* awarded with *Grade Point Average (GPA).* This shall be done by prescribing certain specific thresholds in averages for *Distinction, First Class and Second Class,* as in Table 5.

Table 5: Percentage Equivalence of *Grade Points* (For a 10-Point Scale)

Grade Point	Percentage of Marks / Class
5.75	50 (Second Class)
6.25	55
6.75	60 *(First Class)*
7.25	65
7.75	70 *(First Class with Distinction)*
8.25	75

18. REGISTRATION

Each student has to compulsorily register for course work at the beginning of each semester as per the schedule mentioned in the Academic Calendar. It is absolutely compulsory for the student to register for courses in time.

19. TERMINATION FROM THE PROGRAM

The admission of a student to the program may be terminated and the student is asked to leave the college in the following circumstances:

i. The student fails to satisfy the requirements of the program within the maximum period stipulated for that program.

ii. The student fails to satisfy the norms of discipline specified by the institute from time to time.

20. CURRICULUM

20.1. For each program being offered by the Institute, a Board of Studies (BOS) is constituted in accordance with AICTE / UGC / JNTUH statutes.

20.2. The BOS for a program is completely responsible for designing the curriculum once in three years for that program.

21. WITH-HOLDING OF RESULTS

If the candidate has not paid any dues to the college / if any case of indiscipline / malpractice is pending against him, the results of the candidate will be withheld. The issue of the degree is liable to be withheld in such cases.

22. GRIEVANCES REDRESSAL COMMITTEE

"Grievance and Redressal Committee" (General) constituted by the principal shall deal with all grievances pertaining to the academic / administrative / disciplinary matters. The composition of the complaints cum redressal committee shall be:

Headed by Senior Faculty member
Heads of all departments
A senior lady staff member from each department (if available)

The committee constituted shall submit a report to the principal of the college, the penalty to be imposed. The Principal upon receipt of the report from the committee shall, after giving an opportunity of being heard to the person complained against, submit the case with the committee's recommendation to the Governing Body of the college. The Governing Body shall confirm with or without modification the penalty recommended after duly following the prescribed procedure.

23. MALPRACTICE PREVENTION COMMITTEE

A malpractice prevention committee shall be constituted to examine and punish the students who does malpractice / behaves indiscipline in examinations. The committee shall consist of:

Principal
Subject expert of which the subject belongs to
Head of the department of which the student belongs to
The invigilator concerned
In-charge Examination branch of the college

The committee constituted shall conduct the meeting on the same day of examination or latest by next working day to the incidence and punish the student as per the guidelines prescribed by the J N T University, Hyderabad from time to time.

Any action on the part of candidate at the examination like trying to get undue advantage in the performance at examinations or trying to help another, or derive the same through unfair means is punishable according to the provisions contained hereunder. The involvement of the Staff, who are in charge of conducting examinations, valuing examination papers and preparing / keeping records of documents relating to the examinations in such acts (inclusive of providing incorrect or misleading information) that infringe upon the course of natural justice to one and all concerned at the examination shall be viewed seriously and recommended for award of appropriate punishment after thorough enquiry.

24. AMENDMENTS TO REGULATIONS

The Academic Council of Vardhaman College of Engineering reserves the right to revise, amend, or change the regulations, scheme of examinations, and / or syllabi or any other policy relevant to the needs of the society or industrial requirements etc., without prior notice.

25. STUDENTS' FEEDBACK

It is necessary for the Colleges to obtain feedback from students on their course work and various academic activities conducted. For this purpose, suitable feedback forms shall be devised by the College and the feedback obtained from the students regularly in confidence, by administering the feedback form in print or on-line in electronic form.

The feedback received from the students shall be discussed at various levels of decision making at the College and the changes/ improvements, if any, suggested shall be given due consideration for implementation.

26. GRADUATION DAY

The College shall have its own annual *Graduation Day* for the award of Degrees to students completing the prescribed academic requirements in each case, in consultation with the University and by following the provisions in the Statute.

The College shall institute Prizes and Awards to meritorious students, for being given away annually at the *Graduation Day.* This will greatly encourage the students to strive for excellence in their academic work.

27. AWARD OF A RANK UNDER AUTONOMOUS SCHEME

27.1. One (1) Merit Rank will be declared only for those students who have been directly admitted in VCE under Autonomous Regulations and complete the entire course in VCE only within the minimum possible prescribed time limit, i.e., 2 years for M.Tech.

27.2. A student shall be eligible for a merit rank at the time of award of degree in each branch of Master of Technology, provided the student has passed all subjects prescribed for the particular degree program in first attempt only.

27.5. Award of prizes, scholarships, or any other Honours shall be based on the rank secured by a candidate, consistent with the guidelines of the Donor, wherever applicable.

28. CONDUCT AND DISCIPLINE

28.1 Each student shall conduct himself / herself in a manner befitting his / her association with VCE.

28.2 He / she is expected not to indulge in any activity, which is likely to bring disrepute to the college.

28.3 He / she should show due respect and courtesy to the teachers, administrators, officers and employees of the college and maintain cordial relationships with fellow students.

28.4 Lack of courtesy and decorum unbecoming of a student (both inside and outside the college), wilful damage or removal of Institute's property or belongings of fellow students, disturbing others in their studies, adoption of unfair means during examinations, breach of rules and regulations of the Institute, noisy and unruly behaviour and similar other undesirable activities shall constitute violation of code of conduct for the student.

28.5 **Ragging in any form is strictly prohibited and is considered a serious offence. It will lead to the expulsion of the offender from the college.**

28.6 Violation of code of conduct shall invite disciplinary action which may include punishment such as reprimand, disciplinary probation, debarring from the examination, withdrawal of placement services, withholding of grades / degrees, cancellation of registration, etc., and even expulsion from the college.

28.7 Principal, based on the reports of the warden of Institute hostel, can reprimand, impose fine or take any other suitable measures against an inmate who violates either the code of conduct or rules and regulations pertaining to college hostel.

28.8 A student may be denied the award of degree / certificate even though he / she have satisfactorily completed all the academic requirements if the student is found guilty of offences warranting such an action.

28.9 Attendance is not given to the student during the suspension period.

29. OTHER ISSUES

The quality and standard of engineering professionals are closely linked with the level of the technical education system. As it is now recognized that these features are essential to develop the intellectual skills and knowledge of these professionals for being able to contribute to the society through productive and satisfying careers as *innovators, decision makers and/or leaders* in the global economy of the 21st century, it becomes necessary that certain improvements are introduced at different stages of their education system. These include:

i. Selective admission of students to a programme, so that merit and aptitude for the chosen technical branch or specialization are given due consideration.

ii. Faculty recruitment and orientation, so that qualified teachers trained in good teaching methods, technical leadership and students' motivation are available.

iii. Instructional/Laboratory facilities and related physical infrastructure, so that they are adequate and are at the contemporary level.

iv. Access to good library resources and Information & Communication Technology **(ICT)** facilities, to develop the student's *mind* effectively.

These requirements make it necessary for the College to introduce improvements like:

i. Teaching-learning process on modern lines, to provide *Add-On* Courses for *audit*/credit in a number of peripheral areas useful for students' self development.

ii. Life-long learning opportunities for faculty, students and alumni, to facilitate their dynamic interaction with the society, industries and the world of work.

iii. Generous use of ICT and other modern technologies in everyday activities.

30. GENERAL

Where the words “he”, “him”, “his”, “himself” occur in the regulations, they include “she”, “her”, “herself”.

Note: Failure to read and understand the regulations is not an excuse.

VARDHAMAN COLLEGE OF ENGINEERING
(Autonomous)

SYLLABUS
M. TECH - DIGITAL ELECTRONICS AND COMMUNICATION SYSTEMS

REGULATIONS: VCE--R11

I SEMESTER

Code	Subject	Periods per Week		Credits	Scheme of Examination Maximum Marks		
		L	P		Internal	External	Total
B1401	Advanced Data Communications	3	-	3	40	60	100
B1402	Advanced Digital Signal Processing	3	-	3	40	60	100
B1403	Digital Systems Design	3	-	3	40	60	100
B1404	CMOS VLSI Design	3	-	3	40	60	100
PROFESSIONAL ELECTIVE - I		3	-	3	40	60	100
PROFESSIONAL ELECTIVE - II		3	-	3	40	60	100
B1409	Digital Systems Design Laboratory	-	3	2	40	60	100
B1410	Technical Seminar	-	-	2	50	-	50
TOTAL		**18**	**03**	**22**	**330**	**420**	**750**

II SEMESTER

Code	Subject	Periods per week		Credits	Scheme of Examination Maximum Marks		
		L	P		Internal	External	Total
B1110	Coding Theory and Techniques	3	-	3	40	60	100
B1111	Wireless Communications and Networks	3	-	3	40	60	100
B1411	Low Power CMOS VLSI Design	3	-	3	40	60	100
B1412	Algorithms for VLSI Design Automation	3	-	3	40	60	100
PROFESSIONAL ELECTIVE - III		3	-	3	40	60	100
PROFESSIONAL ELECTIVE - IV		3	-	3	40	60	100
B1418	Advanced Signal Processing and Communications Laboratory	-	3	2	40	60	100
B1419	Technical Seminar	-	-	2	50	-	50
TOTAL		**18**	**03**	**22**	**330**	**420**	**750**

III SEMESTER

Code	Subject	Periods per week		Credits	Scheme of Examination Maximum Marks		
		L	P		Internal	External	Total
B1420	Comprehensive Viva	-	-	4	-	50	50
B1421	Project Work Phase – I	-	-	18	50	-	50
TOTAL		**-**	**-**	**22**	**50**	**50**	**100**

IV SEMESTER

Code	Subject	Periods per week		Credits	Scheme of Examination Maximum Marks		
		L	P		Internal	External	Total
B1422	Project Work Phase – II	-	-	22	50	100	150
TOTAL		**-**	**-**	**22**	**50**	**100**	**150**

VARDHAMAN COLLEGE OF ENGINEERING
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SYLLABUS
M. TECH - DIGITAL ELECTRONICS AND COMMUNICATION SYSTEMS
REGULATIONS: VCE--R11

ELECTIVES			
PROFESSIONAL ELECTIVE - I		**PROFESSIONAL ELECTIVE - II**	
Code	**Subject**	**Code**	**Subject**
B1103	Mobile Satellite Communications	B1105	Optical Communications Technology
B1405	Detection and Estimation Theory	B1407	CPLD and FPGA Architectures and Applications
B1406	Advanced Computer Architecture	B1408	Microcontrollers and Embedded Systems
PROFESSIONAL ELECTIVE - III		**PROFESSIONAL ELECTIVE - IV**	
Code	**Subject**	**Code**	**Subject**
B1413	Network Security and Cryptography	B1115	Optical Networks
B1414	Digital Signal Processors and Architectures	B1416	Design for Testability
B1415	Radar Signal Processing	B1417	Hardware Software Co-Design

VARDHAMAN COLLEGE OF ENGINEERING

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I SEMESTER

ADVANCED DATA COMMUNICATIONS

Course Code: **B1401**

L	P	C
3	-	3

UNIT - I

DIGITAL MODULATION - I: Introduction, information capacity bits, bit rate, baud, and M-ARY coding, ASK, FSK, PSK, QAM methods, band width efficiency, carrier recovery, clock recovery.

UNIT - II

DIGITAL MODULATION - II: QPSK, 8PSK, 16PSK, 8QAM, 16QAM, DPSK methods, band width efficiency, carrier recovery, clock recovery.

UNIT - III

BASIC CONCEPTS OF DATA COMMUNICATIONS, INTERFACES AND MODEMS - I: Data communication, components, networks, distributed processing, network criteria, applications, protocols and standards, standards organizations- regulatory agencies, line configuration- point-to-point and multipoint, topology- mesh, star, tree, bus, ring and hybrid topologies.

UNIT - IV

BASIC CONCEPTS OF DATA COMMUNICATIONS, INTERFACES AND MODEMS - II: transmission modes- simplex- half duplex- full duplex, categories of networks- LAN, MAN, WAN and internetworking, digital data transmission- parallel and serial, DTE- DCE Interface- data terminal equipment, data circuit- terminating equipment, standards EIA 232 interface, other interface standards, modems- transmission rates.

UNIT - V

MULTIPLEXING: Time division multiplexing, T1 digital carrier system, line encoding, T-carriers, frame synchronization, bit interleaving versus word inter leaving, statistical time division multiplexing, wavelength division multiplexing.

UNIT - VI

ERROR DETECTION AND CORRECTION: Types of errors, single bit error, CRC (Cyclic Redundancy Check) performance, checksum, error correction, single bit error correction, hamming code.

DATA LINK CONTROL: Stop and wait, sliding window protocols.

UNIT - VII

DATA LINK PROTOCOLS: Asynchronous protocols, synchronous protocols, character oriented protocol- binary synchronous communication (BSC) - BSC Frames- data transparency, bit oriented protocols – HDLC, link access protocols.

UNIT - VIII

SWITCHING: Circuit switching- space division switches- time division switches- TDM bus- space and time division switching combinations- public switched telephone network, packet switching- datagram approach- virtual circuit approach- circuit switched connection versus virtual circuit connection, message switching.

TEXT BOOKS:

1. B. A. Forouzan (2008), *Data Communication and Computer Networking,* 3rd edition, Tata McGraw Hill publications, New Delhi, India.
2. W. Tomasi (2008), *Advanced Electronic Communication Systems*, 5th edition, Prentice Hall of India, India.

REFERENCE BOOKS:

1. Prakash C. Gupta (2006), *Data Communications and Computer Networks*, Prentice Hall of India, India.
2. William Stallings (2007), *Data and Computer Communications*, 8th edition, Prentice Hall of India, India.
3. T. Housely (2008), *Data Communication and Tele Processing Systems,* 2nd edition, BS Publications, India.

VARDHAMAN COLLEGE OF ENGINEERING

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I SEMESTER

ADVANCED DIGITAL SIGNAL PROCESSING

Course Code: **B1402**

L	P	C
3	-	3

UNIT - I

DESIGN OF DIGITAL FILTERS: Implementation of discrete time systems - IIR and FIR filters.

UNIT - II

MULTIRATE SIGNAL PROCESSING: Introduction, decimation by a factor D, interpolation by a factor I, sampling rate conversion by a rational factor I/D, multistage implementation of sampling rate conversion, filter design & implementation for sampling rate conversion.

UNIT - III

APPLICATIONS OF MULTIRATE SIGNAL PROCESSING: Design of phase shifters, interfacing of digital system with different sampling rates, implementation of narrow band low pass filters, implementation of digital filter banks, sub band coding of speech signals, quadrature mirror filters, transmultiplexers, oversampling A/D and D/A conversion.

UNIT - IV

LINEAR PREDICTION: Forward and backward linear prediction, optimum reflection coefficients for the lattice forward and backward predictors, solution of the normal equations: Levinson Durbin algorithm, Schur algorithm, properties of linear prediction filters.

UNIT - V

NON-PARAMETRIC METHODS OF POWER SPECTRAL ESTIMATION: Estimation of spectra from finite duration observation of signals, non-parametric methods: Bartlett, Welch & Blackman & Tukey methods, comparison of all non-parametric methods.

UNIT - VI

PARAMETRIC METHODS OF POWER SPECTRUM ESTIMATION: Autocorrelation & its properties, relation between auto correlation and model parameters, AR models, Yule Waker and Burg methods, MA and ARMA models for power spectrum estimation.

UNIT - VII

WEINER FILTERS: Linear optimum filtering, principle of orthogonality, minimum mean-square error, Weiner Hopf equations, error performance surface, multiple linear regression model.

UNIT - VIII

KALMAN FILTERS: Statement of Kalman filter, the innovation process, estimation of the state using the innovation process, filtering, initial conditions, summary of Kalman filter.

TEXT BOOKS:

1. J. G. Proakis, D. G. Manolokis (1996), *Digital Signal Processing: Principles, Algorithms & Applications,* 4th edition, Prentice Hall of India, New Delhi.
2. Simon Haykin (2002), *Adaptive Filter Theory,* 4th edition, Pearson Education, New Delhi, India.

REFERENCE BOOKS:

1. S. M. Kay (1988*), Modern spectral Estimation: Theory & Application*, Prentice Hall of India, New Delhi.
2. P. P. Vaidyanathan (2008), *Multirate Systems and Filter Banks,* Pearson Education, New Delhi, India.

VARDHAMAN COLLEGE OF ENGINEERING

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I SEMESTER

DIGITAL SYSTEMS DESIGN

Course Code: **B1403**

L	P	C
3	-	3

UNIT - I

COMBINATIONAL LOGIC DESIGN PRINCIPLES: Introduction, combination circuit analysis, combination circuit synthesis, circuit descriptions and designs, circuit manipulations, combination circuit minimization, Karnaugh maps, minimizing sum of products, programmed minimization methods, timing hazards-static hazards using maps, dynamic hazards, designing hazard free circuits.

UNIT - II

COMBINATIONAL LOGIC DESIGN PRACTICES I: Introduction, timing concepts-timing diagrams, specifications, analysis, analysis tools, propagation delay, combinational; PLDs-PLAs, PLA devices, CPLDs, CMOS PLD circuits, device programming and testing, decoders-binary decoders using HDL.

UNIT - III

COMBINATIONAL LOGIC DESIGN PRACTICES II: Applications of encoders, three state devices, multiplexers, comparators, adders, subtractors and ALUs.

UNIT - IV

SEQUENTIAL LOGIC DESIGN PRINCIPLES: Introduction, latches and flip-flops, clocked synchronous state machine analysis, design, designing state machines using state diagrams, synthesis using transition lists, decomposing state machines using HDL.

UNIT - V

TIMING ISSUES IN SEQUENTIAL LOGIC DESIGN: Introduction, feedback sequential circuit analysis, design, sequential circuit design with HDL, timing issues setup time, hold time and clock skew.

UNIT - VI

DESIGNING WITH PROGRAMMABLE LOGIC DEVICES: Design with FPGA's, one hot state assignment, state transition table, state assignment for FPGA's, problem of initial state assignment for one hot encoding, state machine (SM) charts, derivation of SM charts, realization of SM charts.

UNIT - VII

FAULT MODELING: Logic fault model, fault detection and redundancy, fault equivalence and fault location, fault dominance, single stuck at fault model, multiple stuck at fault models, bridging fault model.

UNIT - VIII

TEST PATTERN GENERATION: Fault diagnosis of combinational circuits by conventional methods, path sensitization techniques, boolean difference method, Kohavi algorithm, test algorithms, D algorithm, PODEM, random testing, transition count testing, signature analysis and test bridging faults.

TEXT BOOKS:

1. John F. Wakerly (2006), *Digital Design Principles and Practices*, 4th Edition, Pearson Education, India.
2. M. L. Bushnell, V. D. Agrawal (2005), *Essentials of Electronic Testing For Digital, Memory and Mixed-Signal VLSI Circuits*, Springer Science, New York.

REFERENCE BOOKS:

1. Miron Abramovici, Melvin A. Breuer, Arthur. D Friedman (1994), *Digital Systems Testing and Testable Design*, IEEE Press, USA.
2. Z. Kohavi (2001) *Switching and Finite Automata Theory*, 2nd Edition, Tata Mc graw Hill, New Delhi.
3. Morris Mano, Michael D. Ciletti (2008), *Digital Design,* 4th Edition, Prentice Hall of India, New Delhi.
4. Samuel C. Lee (1976), *Digital Circuits and Logic Design,* Prentice Hall of India, New Delhi.

VARDHAMAN COLLEGE OF ENGINEERING

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I SEMESTER

CMOS VLSI DESIGN

Course Code: **B1404**

L	P	C
3	-	3

UNIT - I

PHYSICS AND MODELING OF MOSFETS:

Introduction, basic MOSFET characteristics-the MOS threshold voltage & body bias, current-voltage characteristics-square law & bulk charge model, p-channel MOSFETs, MOSFET modeling.

UNIT - II

THE CMOS INVERTER ANALYSIS AND DESIGN: Basic circuit and DC operation-DC characteristics noise margin & layout consideration, inverter switching characteristics-switching intervals, high to low & low to high time, maximum switching frequency, transient effects, RC modeling, propagation delay, output capacitance, inverter design, power dissipation.

UNIT - III

SWITCHING PROPERTIES OF MOSFETS: NFET pass transistors, PMOS transmission characteristics, the inverter revisited series-connected MOSFETs, transient modeling, MOSFET switch logic.

UNIT - IV

STATIC LOGIC CIRCUITS: Complex logic functions, CMOS NAND gate, CMOS NOR gate, complex logic gates, exclusive OR and equivalence gates, adder circuits.

UNIT - V

TRANSMISSION GATE LOGIC CIRCUITS: Basic structure, electrical analysis, RC modeling, TG-based switch logic gates, TG registers, the D-type flip-flop, NFET-based storage circuits, transmission gates in modern design.

UNIT - VI

DYNAMIC LOGIC CIRCUITS: Charge leakage, charge sharing, the dynamic RAM cell, bootstrapping and charge pumps, clocks and synchronization, clocked-CMOS, clock generation circuits,

UNIT - VII

CMOS DYNAMIC LOGIC FAMILIES: Introduction, precharge/evaluate logic, domino logic-gate characteristics, cascades, charge sharing & charge leakage problems, sizing of MOSFET chains, high speed cascades.

UNIT - VIII

CMOS DIFFERENTIAL LOGIC FAMILIES: Dual rail logic, cascode voltage switch logic (CVSL), variations on CVSL logic.

TEXTBOOKS:

1. John P. Uyemura *(*2003*), CMOS Logic Circuit Design*, Kluwer Academic Publishers, USA.
2. Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic (2003), *Digital Integrated Circuits*, 2nd edition, Prentice Hall of India, New Delhi.

REFERENCE BOOKS:

1. Neil Weste, David Harris (2010), *CMOS VLSI Design: A Circuits and Systems Perspective*, 4th edition, Prentice Hall of India, New Delhi.
2. Neil H. E. Weste, Kamran Eshraghian, Michael John Sebastian Smith (2010), *Principles of CMOS VLSI Design: A Systems Perspective with* Verilog*/VHDL Manual*, 2nd edition, Prentice Hall of India, New Delhi.

VARDHAMAN COLLEGE OF ENGINEERING

(Autonomous)

I SEMESTER

MOBILE SATELLITE COMMUNICATIONS

(Professional Elective - I)

Course Code: **B1103**

L	P	C
3	-	3

UNIT - I

INTRODUCTION: Evaluation of mobile telecommunications, satellite system architecture, regulatory considerations, operational considerations, mobile systems, a comparison, related satellite systems.

UNIT - II

SATELLITE ORBITS: Satellite coverage, space environment, eclipse on satellites, suns interface, Doppler effect, orbital debris, summary of orbital characteristics.

UNIT - III

SATELLITE CONSTELLATIONS: Consideration in constellation design, polar constellations, inclined orbit constellations, hybrid constellations, regional coverage, use of spot beams, availability considerations for non geostationary satellites.

UNIT - IV

RADIO LINK: Spectrum sharing methods, spectrum forecast methodology, propagation characteristics, land mobile channel, aeronautical channel, radio link analysis.

UNIT - V

COMMUNICATORS: Gateways, mobile terminals, antennas, hand held communicators, vehicle mounted terminals, biological effects.

UNIT - VI

SPACECRAFT: Satellite for MSS – transponders, antenna systems, effect of orbital altitude on spacecraft design, inter satellite links, launching satellite constellations.

UNIT - VII

REPRESENTATIVE MSS SYSTEMS: Big LEO systems, little LEO systems, MEO systems, hybrid orbit systems.

UNIT - VIII

MOBILE SATELLITE NETWORKS: Operating environment, MSAT network concept, CDMA MSAT network, and statistics of mobile propagation.

TEXT BOOKS:

1. M. Richharia (2003), *Mobile Satellite Communications principles and trends*, Pearson education, India.

REFERENCE BOOKS:

1. Tri T. Ha (1990), *Digital Satellite Communications*, McGraw Hill International Edition, New York.
2. Timothi Pratt, Charles Bostian, Jeremy Allnutt (2003), *Satellite communications*, 2nd edition, Wiley & Sons, New Delhi, India.
3. D. C. Agarwal (1999), *Satellite Communication*, 5th edition, Khanna publication, New Delhi.
4. Gordan L. Stubber (2001), *Principle of Mobile Communication*, 2nd edition, Kluwer academic publishers, USA.

VARDHAMAN COLLEGE OF ENGINEERING

(Autonomous)

I SEMESTER

DETECTION AND ESTIMATION THEORY

(Professional Elective - I)

Course Code: **B1405**

L	P	C
3	-	3

UNIT - I

CLASSICAL DETECTION AND ESTIMATION THEORY: Introduction, simple binary hypothesis tests, M-hypothesis, estimation theory, composite hypothesis.

UNIT - II

REPRESENTATION OF RANDOM PROCESSES: Sampling of band limited random signals, periodic random processes, spectral decomposition, vector random processes.

UNIT - III

DETECTION AND ESTIMATION OF SIGNALS IN WHITE GAUSSIAN NOISE: Introduction, detection of signals in additive white gaussian noise, linear estimation, non linear estimation.

UNIT - IV

DETECTION AND ESTIMATION OF SIGNALS IN NON - WHITE GAUSSIAN NOISE: Whitening approach, a direct derivation using the Karhunen-Loeve expansion, a direct derivation with a sufficient statistic, detection performance, estimation, solution techniques for integral equations, sensitivity, known linear channels, multiple channels and multiple parameter estimation.

UNIT - V

DETECTION OF SIGNALS IN NOISE: Minimum probability error criterion, Neyman-Pearson criterion for radar, detection of variable amplitude signals: matched filters, optimum formulation, detection of random signals.

UNIT - VI

ESTIMATION OF CONTINUOUS WAVEFORMS: Derivation of estimator equations, a lower bound on the mean square estimation error, multi dimensional waveform estimation, nonrandom waveform estimation.

UNIT - VII

RECURSIVE LINEAR MEAN SQUARED ESTIMATION:

TIME VARYING SIGNALS AND KALMAN FILTERING: Introduction, estimation of a signal parameter, recursive estimation of time varying signals, Kalman filtering, filtering signals in noise treatment.

UNIT - VIII

LINEAR ESTIMATION: Realizable linear filters, Kalman Bucy filters, fundamental role of optimum linear filters.

TEXT BOOKS:

1. Harry L. Van Trees (2001), *Detection, Estimation and Modulation Theory*, John Wiley & Sons, USA.
2. Mischa Schwartz, Leonard Shaw (1975), *Signal Processing: Discrete Spectral Analysis, Detection and Estimation*, Mcgrawhill, New Delhi.

REFERENCE BOOKS:

1. Steven. M. Kay (1998), *Fundamentals of Statistical Signal Processing*: Volume- I Estimation Theory, Prentice Hall, USA.
2. Srinath, Rajasekaran, Viswanathan (2003), *Introduction to Statistical Signal Processing with Applications*, Prentice Hall of India, New Delhi.
3. Louis L. Scharf (1991), *Statistical Signal Processing: Detection, Estimation and Time Series Analysis*, Addison Wesley, India.
4. K. Sam Shanmugam, Arthur M. Breiphol (1998), *Random Signals: Detection, Estimation and Data Analysis*, John Wiley & Sons, New Delhi.

VARDHAMAN COLLEGE OF ENGINEERING

(Autonomous)

I SEMESTER

ADVANCED COMPUTER ARCHITECTURE

(Professional Elective - I)

Course Code: **B1406**

L	P	C
3	-	3

UNIT - I

FUNDAMENTALS OF COMPUTER DESIGN: introduction, classes of computers, defining computer architecture, trends in technology, trends in power in integrated circuits, trends in cost, dependability, measuring reporting and summarizing performance.

UNIT - II

INSTRUCTION LEVEL PARALLELISM: Concepts and challenges, basic compiler techniques for exposing ILP, reducing branch costs with prediction, overcoming data hazards with dynamic scheduling, dynamic scheduling: examples and algorithm, hardware based peculation.

UNIT - III

EXPLOITING INSTRUCTION LEVEL PARALLELISM: Exploiting ILP using multiple issue and static scheduling, exploiting ILP using dynamic scheduling , multiple issue and speculation, advanced techniques for instruction delivery and speculation.

UNIT - IV

LIMITS ON INSTRUCTION LEVEL PARALLELISM: Introduction, studies of the limitations of ILP, limitations on ILP for realizable processors, crosscutting issues: hardware versus software speculation, multithreading: using ILP support to exploit thread level parallelism.

UNIT - V

THREAD LEVEL PARALLELISM: introduction, symmetric shared- memory architectures, performance of symmetric shared- memory multiprocessors, distributed shared memory and directory based coherence.

UNIT - VI

SYNCHRONIZATION: The basics, models of memory consistency: an introduction, crosscutting issues.

UNIT - VII

MEMORY HIERARCHY DESIGN: Introduction, eleven advanced optimizations of cache performance, memory technology and optimizations.

UNIT - VIII

PROTECTION: Virtual memory and virtual machines, crosscutting issues: the design of memory hierarchies, AMD memory hierarchy.

TEXT BOOKS:

1. John L. Hennessy, David A. Patterson (2011), *Computer architecture a quantitative approach,* 5th edition, Morgon Kaufmann publishers, USA.
2. Dezso Sima, Terence Fountain, Peter Kacsuk (2009), *Advanced Computer Architecture*, Pearson Education, New Delhi, India.

REFERENCE BOOKS:

1. Kai Hwang, A. Briggs (1998), *Computer Architecture and parallel Processing,* International edition, McGraw Hill, New York, USA.
2. Williams Stallings (1998), *Computer organization and architecture*, Prentice Hall of India, New Delhi, India.

VARDHAMAN COLLEGE OF ENGINEERING

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I SEMESTER

OPTICAL COMMUNICATIONS TECHNOLOGY

(Professional Elective - II)

Course Code: **B1105**

L	P	C
3	-	3

UNIT - I

SIGNAL PROPAGATION IN OPTICAL FIBERS: Geometrical approach and wave theory approach, loss and bandwidth-bending loss, chromatic dispersion-chirped Gaussian pulses and controlling the dispersion profile.

UNIT - II

NONLINEAR EFFECTS OF SIGNAL IN OPTICAL FIBERS: Effective length and area, stimulated Brillouin scattering, stimulated Raman scattering, propagation in a nonlinear medium, self-phase modulation, cross phase modulation, four wave mixing, principle of solitons.

UNIT - III

FIBER OPTIC COMPONENTS - I: Couplers, isolators and circulators, multiplexers and filters, Bragg gratings, Fabry Perot filters, Mach Zehnder interferometers, arrayed waveguide grating and high channel count multiplex architectures.

UNIT - IV

FIBER OPTIC COMPONENTS - II: Optical amplifiers, transmitters, direct and external modulation, pump sources for Raman amplifiers, switches and wavelength converters.

UNIT - V

MODULATION AND DEMODULATION: Signal formats of modulation, subcarrier modulation and multiplexing, optical duobinary modulation, optical single sideband modulation, multilevel modulation, demodulation-ideal receiver, practical direct detection receiver, bit error rates, timing recovery and equalization, error detection and correction-Reed-Solomon codes method.

UNIT - VI

TRANSMISSIONS SYSTEM ENGINEERING - OPTICAL AMPLIFIERS: System model, power penalty, transmitter, receiver, optical amplifiers, crosstalk-types, reduction and cascaded filters, dispersion limits and compensation.

UNIT - VII

TRANSMISSIONS SYSTEM ENGINEERING - FIBER NONLINEARITIES: Effective length in amplified systems, stimulated Brillouin scattering, stimulated Raman scattering, four-wave mixing, self/cross phase modulation, wavelength stabilization.

UNIT - VIII

SYSTEM DESIGN CONSIDERATIONS: Fiber type, chromatic dispersion compensation, modulation, nonlinearities and all-optical networks.

TEXT BOOKS:

1. Rajiv Ramaswami, Kumar N. Sivarajan (2004), *Optical Networks a practical perspective*, 2nd Edition, Morgan Kaufmann Publishers, New Delhi.
2. Gerd Keiser (2000), *Optical Fiber Communications,* 3rd Edition, McGraw Hill, New Delhi.

REFERENCE BOOKS:

1. John. M. Senior (2000), *Optical Fiber Communications: Principles and Practice,* 2nd edition, Pearson Education, New Delhi, India.
2. Govind Agarwal (2004), *Optical Fiber Communications*, 2nd Edition, Tata Mc graw Hill, New Delhi.
3. Harold Kolimbris(2004), *Fiber Optics Communications*, 2nd Edition, Pearson Education, New Delhi, India.
4. Uyless Black (2009), *Optical Networks: third Generation Transport Systems*, 2nd Edition, Pearson Education, New Delhi, India.
5. S. C .Gupta (2004), Optical *Fiber Communications and Its Applications,* Prentice Hall of India, New Delhi.

VARDHAMAN COLLEGE OF ENGINEERING

(Autonomous)

I SEMESTER

CPLD AND FPGA ARCHITECTURES AND APPLICATIONS

(Professional Elective - II)

Course Code: **B1407**

L	P	C
3	-	3

UNIT - I

FPGA BASED SYSTEMS: Introduction, basic concepts, digital design and FPGAs, FPGA based system design.

UNIT - II

FPGA FABRICS: Introduction, FPGA architectures, SRAM based FPGAs, permanently programmed FPGAs.

UNIT - III

FPGA FABRICS II: Chip input/output, circuit design of FPGA fabrics, architecture of FPGA fabrics.

UNIT - IV

COMBINATIONAL LOGIC: Logic design process, combinational network delay, power and energy optimization and arithmetic logic.

UNIT - V

LOGIC IMPLEMENTATION USING FPGAs: Syntax directed translation, logic implementation by macro, logic synthesis, technology independent and dependent logic optimizations, physical design for FPGAs, logic design process revisited.

UNIT - VI

SEQUENTIAL MACHINES: Introduction, sequential machine design process, sequential design styles, rules for clocking, performance analysis.

UNIT – VII

INTRODUCTION TO PLDS: Introduction to PLDs, programmable sum-of-products arrays, PAL fuse matrix and, combinational outputs, PAL outputs with programmable polarity, PAL devices with programmable polarity, universal PAL and generic array logic.

UNIT - VIII

CASE STUDIES: Case studies Xilinx XC4000 and ALTERA's FLEX 8000.

TEXT BOOKS:

1. Wayne Wolf (2004), *FPGA Based System Design*, Pearson Education, New Delhi.
2. Robert Dueck (2000), *Digital design With CPLD Applications and VHDL,* Thomson Learning, USA.

REFERENCE BOOKS:

1. Vikram Arkalgud (2011), *VLSI Design: A Practical Guide for FPGA and ASIC Implementations*, Springer Science, USA.
2. Leo Chartrand (2003), *Advanced Digital Systems: Experiments & Concepts With CPLD's*, Thomson Learning, USA

VARDHAMAN COLLEGE OF ENGINEERING

(Autonomous)

I SEMESTER

MICROCONTROLLERS AND EMBEDDED SYSTEMS

(Professional Elective - II)

Course Code: **B1408**

L	P	C
3	-	3

UNIT - I

INTRODUCTION TO EMBEDDED SYSTEMS: Overview of embedded systems, processor embedded into a system, embedded hardware units and devices in system, embedded software, complex system design, formalization of system design, classification of embedded systems.

UNIT - II

TYPICAL EMBEDDED SYSTEM AND DESIGNING WITH 8-BIT MICROCONTROLLERS: Core of the embedded system, memory, sensors and actuators, communication interfaces, embedded firmware, factors to be considered in selecting controller, designing with 8051, interfacing I/O devices and memory, examples.

UNIT - III

ADVANCED MICROCONTROLLERS: PIC controller's architecture, instruction set, PIC I/O port programming, programming in C.

UNIT - IV

EMBEDDED RISC PROCESSORS: RISC architecture in the PIC, PIC18 pin connections and register configuration, PIC18 timer programming, PIC18 serial port programming in assembly and C.

UNIT - V

EMBEDDED PRODUCT DEVELOPMENT LIFE CYCLE: Embedded product development life cycle: objectives and phases, IDE, types of files generated on cross compilation, disassembler/decompiler, target hardware debugging.

UNIT - VI

INTRODUCTION TO REAL TIME OPERATING SYSTEMS (RTOS): Operating systems basics, types of operating systems tasks, processes, threads and scheduling, multiprocessing and multitasking, task scheduling, task synchronization.

UNIT - VII

VX WORKS AND CASE STUDIES: Real time operating system programming-I, basic functions and types of RTOSes, RTOS mCOS-II,RTOS VxWorks, case studies of programming with RTOS- case study of automatic chocolate vending m/c using μCOS RTOS, case study of sending application layer byte streams on a TCP/IP network.

UNIT - VIII

EMBEDDED SOFTWARE DEVELOPMENT PROCESS AND TOOLS: Introduction to embedded software development process and tools, host and target machines, linking and locating software, getting embedded software into the target system, issues in hardware-software design and co-design, testing - simulation and debugging techniques and tools: testing on host machine , simulators, laboratory tools.

TEXT BOOKS:

1. Raj Kamal (2008), *Embedded Systems - Architecture Programming and Design*, 2nd edition, Tata Mc graw Hill, New Delhi.
2. Shibu K. V (2009), *Introduction to Embedded Systems,* Tata Mc graw Hill, New Delhi.

REFERENCE BOOKS:

1. MD. Ali Mazidi(2009), *PIC Microcontroller and Embedded Systems*, Pearson Education, New Delhi.
2. Steven F. Barrett (2009), *Embedded Systems*, Pearson Education, New Delhi.
3. John B. Peatman (1998), *Designing with PIC Microcontrollers*, Prentice Hall of India, New Delhi.

VARDHAMAN COLLEGE OF ENGINEERING

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I SEMESTER

DIGITAL SYSTEMS DESIGN LABORATORY

Course Code: **B1409**	**L**	**P**	**C**
	-	**3**	**2**

NOTE:

A. Minimum of 12 experiments have to be conducted.

B. All experiments may be simulated using CAD tools and verified on hardware.

LIST OF EXPERIMENTS:

Write VHDL/Verilog program for the following designs and simulate, synthesize, and implement using EDA tools.

1. Basic combinational circuit design – Adders, Multiplexers, Decoders, Encoders and Comparators.
2. Basic sequential circuit design – Flip-flops, Registers and Counters.
3. Generic parallel adder (n - bit Ripple Carry Adder).
4. Carry look ahead adder.
5. Universal shift register.
6. Barrel shifter.
7. Shift register counters
8. Random number generator.
9. Serial data transmitter and serial data receiver.
10. Memory design - ROM and RAM.
11. Stack and Queue implementation using RAM.
12. Frequency divider.
13. String detector/Sequence detector.
14. Digital FIR filter.

VARDHAMAN COLLEGE OF ENGINEERING

(Autonomous)

II SEMESTER

CODING THEORY AND TECHNIQUES

Course Code: **B1110**

L	P	C
3	-	3

UNIT - I

INFORMATION THEORY: Mathematical model of information, a logarithmic measure of information, average and mutual information and entropy types of errors, error control strategies.

LINEAR BLOCK CODES: Introduction to linear block codes, syndrome and error detection, minimum distance of a block code, error detecting and error correcting capabilities of a block code, standard array and syndrome decoding, probability of an undetected error for linear codes over a BSC.

UNIT - II

CYCLIC CODES: Definition of cyclic codes, polynomials, generator polynomials, encoding cyclic codes, decoding cyclic codes, factors of x^n+1, parity check polynomials, dual cyclic codes, generator and parity check matrices of cyclic codes.

UNIT - III

LINEAR FEED BACK SHIFT REGISTERS FOR ENCODING AND DECODING CYCLIC CODES: Linear feedback shift registers, polynomial division register, registers for encoding, registers for error detection and correction, Meggitt decoder, cyclic hamming codes, shortened cyclic codes.

UNIT - IV

CONVOLUTION CODES: Encoding of convolution codes, structural and distance properties of convolutional codes, maximum likelihood decoding- Viterbi decoding.

UNIT - V

SEQUENTIAL AND MAJORITY LOGIC DECODING OF CONVOLUTION CODES: Stack algorithm, Fano algorithm, performance characteristics of sequential decoding, feedback decoding, distance properties and code performance. Application of viterbi decoding and sequential decoding, applications of convolution codes in ARQ system.

UNIT - VI

BURST-ERROR-CORRECTING CODES: Decoding of single burst error correcting cyclic codes, single burst error correcting convolutional codes, bounds on burst error correcting codes, bounds on burst error correcting capability, interleaved cyclic and convolutional codes.

UNIT - VII

GALOIS FIELDS: Roots of equations, Galois fields GF (2^3), Fields GF (2^4) and GF (2^5), primitive field elements, irreducible and primitive polynomials, solution of equations in GF (2^4) and GF (2^3).

UNIT - VIII

BCH CODES: BCH code definition, construction of BCH codes, error syndromes in finite fields, decoding SEC and DEC binary BCH codes, error location polynomial, Peterson- Gorenstein – Zierler decoder, Reed Solomon codes, Berlekamp algorithm, error evaluator polynomial.

TEXT BOOKS:

1. Shu Lin, Daniel J. Costello, Jr(1983), *Error Control Coding Fundamentals and Applications,* Prentice Hall of India, New Delhi.
2. Sal Vatore Gravano (2009), *Introduction to Error Control Codes,* Oxford University Press, USA.

REFERENCE BOOKS:

1. Man Young Rhee (1989), *Error correcting coding theory*, McGraw Hill publishing, New Delhi.
2. Bernard Sklar, Pabitra Kumar Rey *(2009), Digital communications fundamental and application,* 2nd edition, Pearson Education, New Delhi.
3. John G. Proakis (2008), *Digital communications,* 6th edition, Tata Mc graw Hill, New Delhi.

VARDHAMAN COLLEGE OF ENGINEERING

(Autonomous)

II SEMESTER

WIRELESS COMMUNICATIONS AND NETWORKS

Course Code: **B1111**

L	P	C
3	-	3

UNIT - I

WIRELESS COMMUNICATIONS AND SYSTEMS: Introduction to wireless communication systems, examples, comparisons and trends, cellular concepts frequency reuse, channel assignment strategies, handoff strategies, interference and system capacity, trunking & grade of service, improving coverage and capacity in cellular systems.

UNIT - II

MULTIPLE ACCESS TECHNIQUES FOR WIRELESS COMMUNICATIONS: FDMA, TDMA, SSMA (FHMA/CDMA/Hybrid techniques), SDMA techniques (AS applicable to wireless communications), packet radio access-protocols, CSMA, protocols, reservation protocols, capture effect in packet radio, capacity of cellular systems.

UNIT - III

WIRELESS NETWORKING: Introduction, differences between wireless & fixed telephone networks, traffic routing in wireless networks- circuits switching, packet switching, X.25 protocol.

UNIT - IV

WIRELESS DATA SERVICES: Cellular digital packet data (CDPD), advanced radio data information system(ARDIS), RAM mobile data (RMD), common channel signaling (CCS), ISDN-Broadband ISDN and ATM, signaling system no.7 (SS7),network services part of SS7 ,SS7 user part, signaling traffic in SS7,SS7 services, performance of SS7.

UNIT - V

MOBILE IP AND WIRELESS APPLICATION PROTOCOL: Mobile IP, operation of mobile IP, Co-located address, registration, tunneling, WAP architecture, overview, WML scripts, WAP service, WAP session protocol, wireless transaction, wireless datagram protocol.

UNIT - VI

WIRELESS LAN TECHNOLOGY: Infrared LANs, spread spectrum LANs, narrow bank microwave LANs, IEEE 802 protocol architecture, IEEE802 architecture and services. 802.11 medium access control, 802.11 physical layer.

UNIT - VII

BLUE TOOTH: Overview, radio specification, base band specification, links manager specification, logical link control and adaption protocol, introduction to WLL technology.

UNIT - VIII

MOBILE DATA NETWORKS: Introduction, data oriented CDPD network, GPRS and higher data rates, short messaging service in GSM, mobile application protocol.

TEXT BOOKS:

1. Theodore, S. Rappaport (2002), *Wireless communication principles, practice*, 2nd Edition, Prentice Hall of India, New Delhi.
2. William Stallings (2003), *Wireless communication and networking*, Prentice Hall of India, New Delhi.
3. Kaveh Pah Laven, P. Krishna Murthy (2002), *Principles of Wireless networks*, Pearson Education, New Delhi, India.

REFERENCE BOOKS:

1. Kamilo Feher (1999), *Wireless Digital communications*, Prentice Hall of India, New Delhi.
2. Roger I. Freeman (2004), *Telecommunication system engineering*, 4th edition, John Wiley & Son, New Delhi.

VARDHAMAN COLLEGE OF ENGINEERING

(Autonomous)

II SEMESTER

LOW POWER CMOS VLSI DESIGN

Course Code: **B1411**

L	P	C
3	-	3

UNIT - I

PHYSICS OF POWER DISSIPATION: Introduction, sources of power dissipation, MOSFET Devices, power dissipation in CMOS circuits, low-power VLSI design limits.

UNIT - II

POWER ESTIMATION IN CMOS CIRCUITS -I: Introduction, modeling of signals and probability calculations, signal probability using binary decision diagrams, probabilistic techniques for signal activity estimation, switching activity in combinational circuits, derivation of activity for static CMOS circuits, switching activity in sequential circuits and approximation method.

UNIT - III

POWER ESTIMATION IN CMOS CIRCUITS -II: Statistical techniques, combinational and sequential circuits, estimation of glitching power delay models and Monte Carlo techniques, sensitivity analysis, power estimation using input vector compaction and domino CMOS circuits.

UNIT - IV

SYNTHESIS FOR LOW POWER –I: Behavioral level transforms , algorithm level transform , power constrained least squares optimization, architecture driven voltage scaling, power optimization using operation reduction, substitution and pre-computation.

UNIT - V

SYNTHESIS FOR LOW POWER –II: Logic level optimization for low power FSM and combinational logic synthesis, technology mapping, circuit level transforms – introduction, CMOS gates, transistor sizing.

UNIT - VI

LOW POWER STATIC RAM ARCHITECTURES –I: Introduction, organization of static RAM, MOS static RAM memory cell 4T RAM, 6T-RAM cell and advanced RAM architectures.

UNIT - VII

LOW POWER STATIC RAM ARCHITECTURES –II: Banked organization of SRAMs- divided word line architecture, reduced voltage swings on bit lines-pulsed word lines, self-timing the RAM core, pre-charge voltage bit bit-lines, reducing power in the write driver circuits and sense amplifier circuits.

UNIT- VIII

ADVANCED TOPICS: Reversible logic, voltage islands, software design for power estimation – gate level, circuit level and instruction level and power optimization.

TEXT BOOKS:

1. Kaushit Roy, Sharat C. Prasad (2000), *Low Power CMOS VLSI Circuit Design*, Wiley India, New Delhi.
2. Anantha Chandrakasan, Robert W. Brodersen (1998), *Low Power CMOS Design*, IEEE Press, USA.

REFERENCE BOOKS:

1. Christian Piguet (2006), *Low Power CMOS Circuits: Technology, Logic Design and CAD Tools*, CRC Taylor & Francis, New York.
2. Shin ichi Minato (1995), *Binary Decision Diagrams and Applications for VLSI CAD*, The Springer Engineering and Computer International Series, USA.

VARDHAMAN COLLEGE OF ENGINEERING

(Autonomous)

II SEMESTER

ALGORITHMS FOR VLSI DESIGN AUTOMATION

Course Code: **B1412**

L	P	C
3	-	3

UNIT - I

VLSI PHYSICAL DESIGN AUTOMATION: Introduction, VLSI design cycle, new trends in VLSI design cycle, physical design cycle, new trends in physical design cycle, design styles, full custom, standard cell, gate arrays, field programmable gate arrays, sea of gates, comparison of different design styles, system packaging styles, historical perspectives.

UNIT - II

DATA STRUCTURES AND BASIC ALGORITHMS: Basic terminology, complexity issues and NP-hardness, algorithms for NP-hard problems-exponential algorithms, special case algorithms, approximation algorithms, heuristic algorithms, basic algorithms- graph algorithms, computational geometry algorithms, graph algorithms for physical design.

UNIT - III

PARTITIONING: Problem formulation, classification of partitioning algorithms, group migration algorithms, simulated annealing and evolution, metric allocation method.

UNIT - IV

FLOORPLANNING AND PIN ASSIGNMENT: Floorplanning, chip planning, pin assignment, integrated approach.

UNIT - V

PLACEMENT: Problem formulation, classification of placement algorithms, simulation based placement algorithms, partitioning based placement algorithms, other placement algorithms-cluster growth, quadratic assignment, resistive network optimization, branch-and-bound technique.

UNIT - VI

GLOBAL ROUTING: Problem formulation, classification of global routing algorithms, maze routing algorithms, line-probe algorithms, shortest path based algorithms, Steiner tree based algorithms- separability based algorithm, non-rectilinear Steiner tree based algorithm, Steiner Min-Max tree based algorithm, weighted Steiner tree based algorithm.

UNIT - VII

DETAILED ROUTING-I: Problem formulation, classification of routing algorithms, single-layer routing algorithms-general River routing problem, single row routing problem.

UNIT - VIII

DETAILED ROUTING-II: Two-layer channel routing algorithms- classification, LEA based algorithms, constraint graph based routing algorithms, greedy channel router, hierarchical channel router, comparison of two-layer channel routers, three-layer channel routing algorithms - classification, extended net merge channel router, HVH routing from HV solution, Hybrid HVH-VHV router.

TEXT BOOKS:

1. Naveed A. Sherwani(1998), *Algorithms for VLSI Physical Design Automation*, 3rd edition, Kluwer Acadamic Publishers, USA.
2. Sabih H. Gerez (1998), *Algorithms for VLSI Design Automation*, Wiely Publications, New Delhi.

REFERENCE BOOKS:

1. Sung Kyu Lim (2010), *Practical Problems in VLSI Physical Design Automation,* Springer Science, USA.
2. Andrew B. Kahng, Jens Lienig, Igor L. Markov and Jin Hu (2010), *VLSI Physical Design: From Graph Partitioning to Timing Closure*, Springer Science, USA.

VARDHAMAN COLLEGE OF ENGINEERING

(Autonomous)

II SEMESTER

NETWORK SECURITY AND CRYPTOGRAPHY

(Professional Elective - III)

Course Code: **B1413**

L	P	C
3	-	3

UNIT - I

INTRODUCTION SECURITY ATTACKS: Interruption, interception, modification and fabrication.

SECURITY SERVICES: Confidentiality, authentication, integrity, non repudiation, access control and availability.

SECURITY MECHANISMS: A model for internetwork security, internet standards and RFCs, conventional encryption principles, ceaser cipher, hill cipher, poly and mono alphabetic cipher.

UNIT - II

ENCRYPTION PRINCIPLES: Conventional encryption algorithms: Feistal structure, DES algorithm, S: Boxes, Triple DES, advanced data encryption standard (AES), cipher block modes of operation, location of encryption devices, Key distribution Approaches.

UNIT - III

CRYPTOGRAPHY AND APPLICATIONS : Public key cryptography principles, public key cryptography algorithms, digital signatures, RSA, elliptic algorithms, digital certificates, certificate authority and key management, Kerberos, X.509, directory authentication service. Message authentication, secure hash functions and HMAC.

UNIT - IV

ELECTRONIC MAIL SECURITY: Email privacy, PGP operations, radix: 64 conversions, key management for PGP, PGP trust model, multipurpose internet mail extension (MIME), secure/MIME(S/MIME).

UNIT - V

IP SECURITY ARCHITECTURE AND SERVICES: IP security overview, IP security architecture, security association, authentication header, encapsulating security payload, combining security associations and key management, OAKELY key determination protocol, ISAKMP.

UNIT - VI

WEB SECURITY: Web security considerations, secure socket layer (SSL) and transport layer security (TLS), secure electronic transaction (SET).

UNIT - VII

NETWORK MANAGEMENT SECURITY: Basic concepts of SNMP, SNMPv1 community facility and SNMPv3. System Security, intruders, intrusion techniques, intrusion detection, password management, bot nets.

UNIT - VIII

MALICIOUS SOFTWARE: Viruses and related threats, virus counter measures, distributed denial of service attacks.

FIREWALLS: Firewall design principles, trusted systems, common criteria for information technology security evolution.

TEXT BOOKS:

1. William Stallings (2007), *Network Security Essentials (Applications and Standards*), 3rd Edition, Pearson Education, New Delhi, India.
2. William Stallings (1998), *Cryptography and network Security*, 3rd Edition, Prentice Hall of India, New Delhi, India.

REFERENCE BOOKS:

1. Eric Maiwald (2004), *Fundamentals of Network Security*, Dreamtech press, India.
2. Charlie Kaufman, Radia Perlman, Mike Speciner (2002), *Network Security: Private Communication in a Public World*, 2nd Edition, Pearson Education, India.
3. Robert Bragg, Mark Rhodes (2004), *Network Security: The Complete Reference*, Tata Mcgraw Hill, New Delhi.
4. Buchmann (2004), *Introduction to Cryptography*, 2nd Edition, Springer, USA.

VARDHAMAN COLLEGE OF ENGINEERING

(Autonomous)

II SEMESTER

DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES

(Professional Elective - III)

Course Code: **B1414**

L	P	C
3	-	3

UNIT - I

INTORODUCTION TO DIGITAL SIGNAL PROCESING: Introduction, digital signal-processing system, the sampling process, discrete time sequences. discrete Fourier transform (DFT) and fast Fourier transform (FFT), linear time-invariant systems, digital filters, decimation and interpolation, analysis and design tool for DSP systems MATLAB, DSP using MATLAB.

UNIT - II

COMPUTATIONAL ACCURACY IN DSP IMPLEMENTATIONS: Number formats for signals and coefficients in DSP systems, dynamic range and precision, sources of error in DSP implementations, A/D conversion errors, DSP computational errors, D/A conversion errors, compensating filter.

UNIT - III

ARCHITECTURES FOR PROGRAMMABLE DSP DEVICES: Basic architectural features, DSP computational building blocks, bus architecture and memory, data addressing capabilities, address generation unit, programmability and program execution, speed issues, features for external interfacing.

UNIT - IV

EXECUTION CONTROL AND PIPELINING: Hardware looping, interrupts, stacks, relative branch support, pipelining and performance, pipeline depth, interlocking, branching effects, interrupt effects, and pipeline programming models.

UNIT - V

PROGRAMMABLE DIGITAL SIGNAL PROCESSORS : Commercial digital signal-processing devices, data addressing modes of TMS320C54XX DSPs, data addressing modes of TMS320C54XX processors, memory space of TMS320C54XX processors, program control, TMS320C54XX instructions and programming, on-chip peripherals, interrupts of TMS320C54XX processors, pipeline operation of TMS320C54XX processors.

UNIT - VI

IMPLEMENTATIONS OF BASIC DSP ALGORITHMS: The Q-notation, FIR filters, IIR filters, interpolation filters, decimation filters, PID controller, adaptive filters, 2-D signal processing.

UNIT - VII

IMPLEMENTATION OF FFT ALGORITHMS : An FFT algorithm for DFT computation, a Butterfly computation, overflow and scaling, bit-reversed index generation, an 8-Point FFT implementation on the TMS320C54XX, computation of the signal spectrum.

UNIT - VIII

INTERFACING MEMORY AND I/O PERIPHERALS TO PROGRAMMABLE DSP DEVICES: Memory space organization, external bus interfacing signals, memory interface, parallel I/O interface, programmed I/O, interrupts and I/O, direct memory access (DMA). a multichannel buffered serial port (McBSP), McBSP programming, a CODEC interface circuit, CODEC programming, a CODEC-DSP interface example.

TEXT BOOKS:

1. Avtar Singh, S. Srinivasan (2004), *Digital Signal Processing Implementations*, Thomson Publications, New Delhi.
2. Lapsleyetal. S (2000), *DSP Processor Fundamentals, Architectures & Features, S.* Chand & Co, New Delhi.

REFERENCE BOOKS:

1. B. Venkata Ramani, M. Bhaskar (2004), *Digital Signal Processors, Architecture, Programming and Applications*, Tata Mcgraw Hill, New Delhi.
2. Jonatham Stein (2005), *Digital Signal Processing,* John Wiley, New Delhi.

VARDHAMAN COLLEGE OF ENGINEERING

(Autonomous)

II SEMESTER

RADAR SIGNAL PROCESSING

(Professional Elective - III)

Course Code: **B1415**

L	P	C
3	-	3

UNIT - I

INTRODUCTION: Radar block diagram, radar equation, information available from radar echo. Review of radar range performance, general radar range equation, radar detection with noise jamming, Beacon and repeater equations, bistatic radar.

UNIT - II

MATCHED FILTER RECEIVER: Impulse response, frequency response characteristic and its derivation, matched filter and correlation function, correlation detection and cross-correlation receiver, efficiency of non-matched filters, matched filter for non-white noise.

UNIT - III

DETECTION OF RADAR SIGNALS IN NOISE: Detection criteria, Neyman - Pearson observer, likelihood-ratio receiver, inverse probability receiver, sequential observer, detectors – envelope detector, logarithmic detector, I/Q detector, automatic detection, CFAR Receiver, cell averaging CFAR receiver, CFAR loss, CFAR uses in radar, radar signal management – schematics, component parts, resources and constraints.

UNIT - IV

WAVEFORM SELECTION: Radar ambiguity function and Ambiguity Diagram – principles and properties; specific cases – ideal case, single pulse of sine wave, periodic pulse train, single linear FM pulse, noise like waveforms.

UNIT - V

WAVEFORM DESIGN REQUIREMENTS: Optimum waveforms for detection in clutter, family of radar waveforms, generation and decoding of FM waveforms – block schematic and characteristics of passive system, digital compression, SAW pulse compression.

UNIT - VI

PULSE COMPRESSION IN RADAR SIGNALS: Introduction, significance, types, linear FM pulse compression – block diagram, characteristics, reduction of time sidelobes, stretch techniques,

UNIT - VII

PHASE CODING TECHNIQUES: Principles, binary phase coding, barker codes, maximal length sequences (MLS/LRS/PN), block diagram of phase coded CW radar.

UNIT - VIII

POLY PHASE CODES: Frank codes, Costas codes, non-linear FM pulse compression, Doppler tolerant PC waveforms – short pulse, linear period modulation (LPM/HFM), side lobe reduction for phase coded PC signals.

TEXT BOOKS:

1. M. I. Skolnik (1991), *Radar Handbook*, 2nd edition, Tata McGraw Hill, New Delhi.
2. Fred E. Nathanson (1999), *Radar Design Principles: Signal Processing and the Environment,* 2nd edition, Prentice Hall of India, New Delhi.
3. M.I. Skolnik (2001), *Introduction to Radar Systems*, 3rd edition, Tata Mcgraw Hill, New Delhi.

REFERENCE BOOKS:

1. Z. Peebles, Jr (2004), *Radar Principles,* John Wiley, New Delhi.
2. R. Nitzberg (1999), *Radar Signal Processing and Adaptive Systems*, Artech House, Boston.
3. F. E. Nathanson (1969), *Radar Design Principles*, 1st edition, Tata McGraw Hill, New Delhi.

VARDHAMAN COLLEGE OF ENGINEERING

(Autonomous)

II SEMESTER

OPTICAL NETWORKS

(Professional Elective - IV)

Course Code: **B1115**

L	P	C
3	-	3

UNIT - I

CLIENT LAYERS OF THE OPTICAL NETWORKS: SONET/SDH – multiplexing, frame structure, physical layer, infrastructure, ATM – functions, adaptation layers, QoS, flow control, Signaling and Routing, IP- routing and forwarding, QoS, MPLS, storage area networks - ESCON, fiber channel, HIPPI and Gigabit ethernet.

UNIT - II

WDM NETWORK ELEMENTS: Optical Line terminals and amplifiers, Add/Drop Multiplexers- OADM Architecture and reconfigurable OADMS, Optical cross connects, all-optical OXC configurations.

UNIT - III

WDM NETWORK DESIGN: Cost tradeoffs in network design, LTD and RWA problems, dimensioning wavelength routing networks, statistical and maximum load dimensioning models.

UNIT - IV

NETWORK CONTROL AND MANAGEMENT: Network management functions, optical layer services and interfacing, layers within optical layer, multivendor interoperability, performance and fault management, configuration management and optical safety.

UNIT - V

NETWORK SURVIVABILITY: Basic concepts, protection in SONET/SDH links and rings, protection in IP networks, optical Layer protection – service classes, protection schemes and Interworking between layers.

UNIT - VI

ACCESS NETWORKS: Network architecture, enhanced HFC, FTTC- PON evolution.

UNIT - VII

PHOTONIC PACKET SWITCHING: OTDM, synchronization, header processing, buffering, burst switching and test beds.

UNIT - VIII

DEPLOYMENT CONSIDERATIONS: SONET/SDH core network, architectural choices for next generation transport networks, designing the transmission layer using SDM, TDM and WDM, unidirectional and bidirectional WDM systems, long haul and metro networks.

TEXT BOOKS:

1. Rajiv Ramaswami, Kumar N. Sivarajan (2004), *Optical Networks a practical perspective*, 2nd edition, Morgan Kaufmann Publishers.
2. C. Siva Rama Murthy, Mohan Guruswamy (2003), *WDM Optical Networks: Concepts, Design and Algorithms,* 2nd edition, Pearson Education, New Delhi, India.

REFERENCE BOOKS:

1. Uyless Black (2009), *Optical Networks: third Generation Transport Systems*, 2nd edition, Pearson Education, New Delhi, India.
2. John. M. Senior (2000), *Optical Fiber Communications: Principles and Practice,* 2nd edition, Pearson Education, New Delhi, India.
3. Harold Kolimbris (2004), *Fiber Optics Communications*, 2nd edition, Pearson Education, New Delhi, India.
4. Timothy S. Ramteke (2004), *Networks*, 2nd edition, Pearson Education, New Delhi, India.
5. Govind Agarwal (2004), *Optical Fiber Communications*, 2nd edition, Tata Mc graw Hill, New Delhi.
6. S. C. Gupta (2004), *Optical Fiber Communications and Its Applications,* Prentice Hall of India, India.
7. Roger L. Freeman (2004), *Telecommunication System Engineering,* John Wiley and Sons, New Delhi.

VARDHAMAN COLLEGE OF ENGINEERING

(Autonomous)

II SEMESTER

DESIGN FOR TESTABILITY

(Professional Elective - IV)

Course Code: **B1416**

L	P	C
3	-	3

UNIT - I

INTRODUCTION TO TEST AND DESIGN FOR TESTABILITY (DFT) FUNDAMENTALS: Modeling: modeling digital circuits at logic level, register level, and structural models, levels of modeling.

UNIT - II

LOGIC SIMULATION: Types of simulation, delay models, element evaluation, hazard detection. Gate level event driven simulation.

UNIT - III

FAULT MODELING: Logic fault models: fault detection and redundancy, fault equivalence and fault location, single stuck and multiple stuck-fault models, fault simulation applications, general techniques for combinational circuits.

UNIT - IV

STUCK AT FAULT MODELS: Testing for single stuck faults (SSF) – automated test pattern generation (ATPG/ATG) for SSFs in combinational and sequential circuits, functional testing with specific fault models, vector simulation – ATPG vectors, formats, compaction and compression, selecting ATPG tool.

UNIT - V

DESIGN FOR TESTABILITY: Testability tradeoffs techniques scan architectures and testing, controllability and absorbability, generic boundary scan, fully integrated scan, storage cells for scan design, board level and system level approaches, boundary scans standards.

UNIT - VI

COMPRESSIONS TECHNIQUES: Different techniques, syndrome test and signature analysis.

UNIT - VII

BUILT-IN SEFT TEST (BIST): BIST concepts and test pattern generation, specific BIST architectures LOCST, STUMPS, CBIST, RTD, BILBO, brief ideas on some advanced BIST concepts and design for self test at board level.

UNIT - VIII

MEMORY BIST (MBIST): Memory test architectures and techniques, introduction to Memory test, types of memories and integration, embedded memory testing model, memory test requirements for MBIST, JTAG testing features.

TEXT BOOKS:

1. Miron Abramovici, Melvin A. Breur, Arthu D. Friedman (1994), *Digital Systems Testing and Testable Design,* John Wiley & sons., New Delhi
2. Alfred Crouch (2008), *Design for Test for Digital ICs & Embedded Core Systems,* Pearson Education, New Delhi, India.

REFERENCE BOOKS:

1. Robrt. J. Feugate, J. Steven M. Mclntyre, Englehood Cliffs (1988), *Introduction to VLSI Testing,* Prentice Hall of India, New Delhi.
2. M.L. Bushnell, Vishwani. D. Agarwal (2004), *Essentials of Electronic Testing,* Springer Science, USA.

VARDHAMAN COLLEGE OF ENGINEERING

(Autonomous)

II SEMESTER

HARDWARE SOFTWARE CO-DESIGN

(Professional Elective - IV)

Course Code: **B1417**

L	P	C
3	-	3

UNIT - I

CO DESIGN ISSUES: Co- design models, architectures, languages, and a generic co-design methodology.

UNIT - II

CO SYNTHESIS ALGORITHMS: Hardware software synthesis algorithms, hardware – software partitioning distributed system co-synthesis.

UNIT - III

PROTOTYPING AND EMULATION: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure.

UNIT - IV

TARGET ARCHITECTURES: Architecture specialization techniques, system communication infrastructure, target architecture and application system classes, architecture for control dominated systems (8051-architectures for high performance control), architecture for data dominated systems (ADSP21060, TMS320C60), mixed systems.

UNIT - V

COMPILATION TECHNIQUES AND TOOLS FOR EMBEDDED PROCESSOR ARCHITECTURES: Modern embedded architectures, embedded software development needs, compilation technologies practical consideration in a compiler development environment.

UNIT - VI

DESIGN SPECIFICATION AND VERIFICATION: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification.

UNIT - VII

LANGUAGES FOR SYSTEM – LEVEL SPECIFICATION AND DESIGN-I: System – level specification, design representation for system level synthesis, system level specification languages.

UNIT - VIII

LANGUAGES FOR SYSTEM – LEVEL SPECIFICATION AND DESIGN-II: Heterogeneous specifications and multi language co-simulation the Cosyma system and Lycos system.

TEXT BOOKS:

1. Jorgen Staunstrup, Wayne Hendrix Wolf (2002), *Hardware / software co- design Principles and Practice*, kluwer academic publishers, USA.

REFERENCE BOOKS:

1. Patrick R. Schaumont (2010), *A Practical Introduction to Hardware/Software Do-design*, Springer.
2. Giovanni De Micheli, Mariagiovanna Sami (1996), *Hardware/Software Co-design*, Kluwer Academic.

VARDHAMAN COLLEGE OF ENGINEERING

(Autonomous)

II SEMESTER

ADVANCED SIGNAL PROCESSING AND COMMUNICATIONS LABORATORY

Course Code: **B1418**	**L**	**P**	**C**
	-	**3**	**2**

NOTE:

A. Minimum of 12 Experiments have to be conducted, 6 experiments from each part.

B. All Experiments may be simulated using MATLAB and to be verified using related trainer kits.

LIST OF EXPERIMENTS:

PART - A:

1. Basic operations on signals, generation of various signals, and finding its FFT and IFFT of a given sequence.
2. Program to verify decimation and interpolation of a given sequences.
3. Design of FIR filter using windowing techniques.
4. Implementation of linear and circular convolution.
5. Generation of Dual Tome Multiple Frequency (DTMF) signals.
6. a) Estimation of power spectrum using Bartlett and Welch method.
   b) Estimation of power spectrum using Blackman-Tukey method.
7. Verification of Autocorrelation theorem.
8. Parametric methods (Yule-Walker and Burg) of power spectrum estimation.
9. Estimation of data series using n^{th} order Forward Predictor and comparing to the original signal.

PART - B:

1. Characterization of LED.
2. Determination of numerical aperture of given optical fibers.
3. Determination of losses in optical fibers.
4. Measurement of bit error rate using binary data.
5. Verification of minimum distance in Hamming code.
6. Error detection and correction by convolutional codes.
7. Efficiency of DS Spread – spectrum technique.
8. Simulation of Frequency Hopping (FH) system.
9. Effect of sampling and quantization of digital image.

M. Tech. DECS I / II SEMESTER

TECHNICAL SEMINAR

L	T	P	C
-	-	-	2

1. OBJECTIVE:

Seminar is an important component of learning in an Engineering College, where the student gets acquainted with preparing a report & presentation on a topic.

2. **PERIODICITY / FREQUENCY OF EVALUATION: Twice**

3. PARAMETERS OF EVALUATION:

1. The seminar shall have two components, one chosen by the student from the course-work without repetition and approved by the faculty supervisor. The other component is suggested by the supervisor and can be a reproduction of the concept in any standard research paper or an extension of concept from earlier course work.
2. The two components of the seminar are distributed between two halves of the semester and are evaluated for 50 marks each. The average of the two components shall be taken as the final score.
3. The students shall be required to submit the rough drafts of the seminar outputs within one week of the commencement of the class work.
4. Supervisor shall make suggestions for modification in the rough draft. The final draft shall be presented by the student within a week thereafter.
5. Presentation schedules will be prepared by different Departments in line with the academic calendar.

The Seminars shall be evaluated in two stages as follows:

A. Rough draft

In this stage, the student should collect information from various sources on the topic and collate them in a systematic manner. He/ She may take the help of the concerned supervisor.

The report should be typed in “MS-Word” file with “calibri” font, with font size of 16 for main heading, 14 for sub-headings and 11 for the body text. The contents should also be arranged in Power Point Presentation with relevant diagrams, pictures and illustrations. It should normally contain 18 to 25 slides, consisting of the followings:

1.	Topic, name of the student & guide	1 Slide
2.	List of contents	1 Slide
3.	Introduction	1 - 2 Slides
4.	Descriptions of the topic (point-wise)	7 - 10 Slides
5.	Images, circuits etc.	6 - 8 Slides
6.	Conclusion	1 - 2 Slides
7.	References/Bibliography	1 Slide

The soft copy of the rough draft of the seminar presentation in MS Power Point format along with the draft Report should be submitted to the concerned supervisor, with a copy to the concerned HOD within 30 days of the commencement of class work.

The evaluation of the Rough draft shall generally be based upon the following.

1.	Punctuality in submission of rough draft and discussion	2 Marks
2.	Resources from which the seminar have been based	2 Marks
3.	Report	3 Marks
4.	Lay out, and content of Presentation	3 Marks
5.	Depth of the students knowledge in the subject	5 Marks
Total		15 Marks

After evaluation of the first draft the supervisor shall suggest further reading, additional work and fine tuning, to improve the quality of the seminar work.

Within 7 days of the submission of the rough draft, the students are to submit the final draft incorporating the suggestions made by the supervisor.

B. Presentation:

After finalization of the final draft, the students shall be allotted dates for presentation (in the designated seminar classes) and they shall then present it in presence students, supervisor, faculties of the department and at least one faculty from some department / other department.

The student shall submit 3 copies of the Report neatly bound along with 2 soft copies of the PPT in DVD medium. The students shall also distribute the title and abstract of the seminar in hard copy to the audience. The final presentation has to be delivered with 18-25 slides.

The evaluation of the Presentation shall generally be based upon the following.

1.	Contents	10 Marks
2.	Delivery	10 Marks
3.	Relevance and interest the topic creates	5 Marks
4.	Ability to involve the spectators	5 Marks
5.	Question answer session	5 Marks
Total		35 Marks

4. WHO WILL EVALUATE?

The presentation of the seminar topics shall be made before an internal evaluation committee comprising the Head of the Department or his/her nominee, seminar supervisor and a senior faculty of the department / other department.

M. Tech. DECS III SEMESTER

COMPREHENSIVE VIVA

Course Code: **B1420**

L	T	P	C
-	-	-	4

1. OBJECTIVE:

- To enable the examiners to assess the candidate's knowledge in his or her particular field of learning.
- To test the student's awareness of the latest developments and relate them to the knowledge acquired during the classroom teaching.

2. PARAMETERS OF EVALUATION:

Subject Knowledge	Current Awareness	Career Orientation	Communication Skills	Total
20	10	10	10	50

3. WHO WILL EVALUATE?

The comprehensive Viva will be conducted by a committee comprising Head of the Department or his/her nominee, two senior faculty of the respective department and an external examiner from outside the college. The comprehensive viva shall be evaluated for 50 marks at the end of III semester. A minimum of 40% of maximum marks shall be obtained to earn the corresponding credits.

4. **PERIODICITY / FREQUENCY OF EVALUATION: Once**

5. PEDAGOGY:

- The viva will be held on a face to face basis.
- The students will be expected to answer the questions related to latest developments and all courses taken till date.
- Viva voce will be conducted within week before the beginning of midterm examinations. However, in exceptional circumstances it can be scheduled immediately after the end of midterm examinations.
- Students will have to make themselves available on the date of the viva voce.

M. Tech. DECS III/ IV SEMESTER

PROJECT WORK

1. OBJECTIVE:

The main objective of the Project Work is for the students to learn and experience all the major phases and processes involved in solving "real life engineering problems".

2. EXPECTED OUTCOME:

The major outcome of the M. Tech project must be well-trained students. More specifically students must have acquired:

- System integration skills
- Documentation skills
- Project management skills
- Problem solving skills

3. PROJECT SELECTION:

Projects are suggested by the faculty, with or without collaboration with an industry. All faculty are to suggest projects. Students are also encouraged to give project proposals after identifying a faculty who would be willing to supervisor the work. A Project brief is to be given by the faculty to the group defining the project comprehensively.

All M. Tech major projects are to be done in the Institute. For industry specified projects, students will be permitted to spend 1-2 weeks in the industry on recommendation by the supervisor. The number of students per batch should be 1.

4. WHO WILL EVALUATE?

The end semester examination shall be based on the report submitted and a viva-voce exam for 100 marks by committee comprising of the Head of the Department, project supervisor and an external examiner.

5. EVALUATION:

The basic purpose is to assess the student competencies with regard to his project work. More specifically to assess the student's individual contribution to the project, to establish the level of understanding of basic theoretical knowledge relevant to the project and to ensure that the student has good understanding and appreciation of design and development decisions taken in the course of the project. It is desirable that all faculty members are present for the evaluations as this is a platform to get to know the student projects and to motivate the students to do good projects. The faculty should adopt a clear and consistent pattern of asking questions from general to specific aspects of the project. The presentation and evaluation is open to other students of the department.

The project work shall be evaluated for 150 marks out of which 50 marks for internal evaluation and 100 marks for end-semester evaluation. The evaluation shall be done on the following basis

Semester III	**Semester IV**
Preliminary Evaluation - 50 marks	Design Evaluation I - 25 marks
	Design Evaluation II - 25 marks
	Final Evaluation – 100 marks

6. GUIDELINES FOR THE PREPARATION OF M. TECH PROJECT REPORTS

1.1. Project reports should be typed neatly only on one side of the paper with 1.5 or double line spacing on a A4 size bond paper (210 x 297 mm). The margins should be: Left - 1.25", Right - 1", Top and Bottom - 0.75".

1.2. The total number of reports to be prepared are:

- One copy to the department

- One copy to the concerned guide(s)
- One copy to the candidate.

1.3. Before taking the final printout, the approval of the concerned guide(s) is mandatory and suggested corrections, if any, must be incorporated.

1.4. For making copies dry tone Xerox is suggested.

1.5. Every copy of the report must contain

- Inner title page (White)
- Outer title page with a plastic cover
- Certificate in the format enclosed both from the college and the organization where the project is carried out.
- An abstract (synopsis) not exceeding 100 words, indicating salient features of the work.

6.6. The organization of the report should be as follows:

1.	Inner title page	Usually numbered in roman
2.	Abstract or Synopsis	
3.	Acknowledgments	
4.	Table of Contents	
5.	List of table & figures (optional)	

6.7 Chapters (to be numbered) containing Introduction, which usually specifies the scope of work and its importance and relation to previous work and the present developments, Main body of the report divided appropriately into chapters, sections and subsections.

- The chapters, sections and subsections may be numbered in the decimal form for e.g. Chapter 2, sections as 2.1, 2.2 etc., and subsections as 2.2.3, 2.5.1 etc.
- The report should be typed in "MS-Word" file with "calibri" font. The chapter must be left or right justified (font size 16). Followed by the title of chapter centered (font size 18), section/subsection numbers along with their headings must be left justified with section number and its heading in font size 16 and subsection and its heading in font size 14. The body or the text of the report should have font size 11.
- The figures and tables must be numbered chapter wise for e.g.: Fig. 2.1 Block diagram of a serial binary adder, Table 3.1 Primitive flow table, etc.
- The last chapter should contain the summary of the work carried, contributions if any, their utility along with the scope for further work.

6.8. Reference OR Bibliography: The references should be **numbered serially** in the order of their occurrence in the text and their numbers should be indicated within square brackets for e.g. [3]. The section on references should list them in serial order in the following format.

1. For textbooks - A.V. Oppenheim and R.W. Schafer, Digital Signal Processing, Englewood, N.J., Prentice Hall, 3 Edition, 1975.
2. For papers - Devid, Insulation design to combat pollution problem, Proc of IEEE, PAS, Vol 71, Aug 1981, pp 1901-1907.

6.9. Only SI units are to be used in the report. Important equations must be numbered in decimal form for e.g. **V = IZ** ..... **(3.2)**

6.10. All equation numbers should be right justified.

6.11. The project report should be brief and include descriptions of work carried out by others only to the minimum extent necessary. Verbatim reproduction of material available elsewhere should be strictly avoided. Where short excerpts from published work are desired to be included, they should be within quotation marks appropriately referenced.

6.12. Proper attention is to be paid not only to the technical contents but also to the organization of the report and clarity of the expression. Due care should be taken to avoid spelling and typing errors. The student should note that report-write-up forms the important component in the overall evaluation of the project

6.13. Hardware projects must include: the component layout, complete circuit with the component list containing the name of the component, numbers used, etc. and the main component data sheets as Appendix. At the time of report submissions, the students must hand over a copy of these details to the project coordinator and see that they are entered in proper registers maintained in the department.

6.14. Software projects must include a virus free disc, containing the software developed by them along with the read me file. Read me file should contain the details of the variables used, salient features of the software and procedure of using them: compiling procedure, details of the computer hardware/software requirements to run the same, etc. If the developed software uses any public domain software downloaded from some site, then the address of the site along with the module name etc. must be included on a separate sheet. It must be properly acknowledged in the acknowledgments.

6.15. Sponsored Projects must also satisfy the above requirements along with statement of accounts, bills for the same dully attested by the concerned guides to process further, They must also produce NOC from the concerned guide before taking the internal viva examination.

6.16. The reports submitted to the department/guide(s) must be hard bounded, with a plastic covering.

6.17. Separator sheets, used if any, between chapters, should be of thin paper

VARDHAMAN COLLEGE OF ENGINEERING

(Autonomous)

Shamshabad – 501 218, Hyderabad

Department of ……..

CERTIFICATE

Certified that the project work entitled …….. carried out by Mr./Ms. ……., Roll Number ……., a bonafide student of ……in partial fulfillment for the award of **Master of Technology** in …… of the Jawaharlal Nehru Technological University, Hyderabad during the year …….. It is certified that all corrections / suggestions indicated for Internal Assessment have been incorporated in the Report deposited in the departmental library. The project report has been approved as it satisfies the academic requirements in respect of Project work prescribed for the said Degree.

Name & Signature of the Guide **Name Signature of the HOD** **Signature of the Principal**

External Viva

Name of the examiners Signature with date

1.

2.

Certificate issued at the Organization where the project was carried out

(On a separate sheet, If applicable)

NAME OF THE INDUSTRY / ORGANIZATION, Address with pin code

CERTIFICATE

Certified that the project work entitled …….. carried out by Mr./Ms . ……., Roll Number……., a bonafide student of ……in partial fulfillment for the award of **Master of Technology** in …… of the Jawaharlal Nehru Technological University, Hyderabad during the year …….. It is certified that, he/she has completed the project satisfactorily

Name & Signature of the Guide **Name & Signature of the Head of Organization**

7. **DISTRIBUTION OF MARKS FOR M.TECH DISSERTATION EVALUATION**

S No.	Particulars	Max. Marks
1	Relevance of the subject in the present context	**10**
2	Literature Survey	**10**
3	Problem formulation	**10**
4	Experimental observation / theoretical modeling	**10**
5	Results – Presentation & Discussion	**20**
6	Conclusions and scope for future work	**10**
7	Overall presentation of the Thesis / Oral presentation	**20**
8	Project Report Writing	**10**
Total Marks		**100**

MALPRACTICES RULES
DISCIPLINARY ACTION FOR / IMPROPER CONDUCT IN EXAMINATIONS

	Nature of Malpractices/Improper conduct	Punishment
	If the candidate:	
1. (a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination)	Expulsion from the examination hall and cancellation of the performance in that subject only.
(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2.	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that Semester/year. The Hall Ticket of the candidate is to be cancelled and sent to the University.
3.	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred and forfeits the seat. The performance of the original candidate, who has been impersonated, shall be cancelled in all the subjects of the examination (including practicals and project work) already appeared and shall not be allowed to appear for examinations of the remaining subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.
4.	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5.	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that subject.
6.	Refuses to obey the orders of the Chief Superintendent/Assistant – Superintendent / any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in charge or any person on duty in or outside the examination hall of any injury to his person or to	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The candidates also are debarred and forfeit their

	any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer-in-charge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	seats. In case of outsiders, they will be handed over to the police and a police case is registered against them.
7.	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
8.	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat.
9.	If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	Student of the colleges expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the College will be handed over to police and, a police case will be registered against them.
10.	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year.
11.	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester/year examinations.
12.	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the University for further action to award suitable punishment.	

Frequently asked Questions and Answers about autonomy

1. Who grants Autonomy? UGC, Govt., AICTE or University

In case of Colleges affiliated to a university and where statutes for grant of autonomy are ready, it is the respective University that finally grants autonomy.

2. Shall VCE award its own Degrees?

No. Degree will be awarded by Jawaharlal Nehru Technological University, Hyderabad with a mention of the name Vardhaman College of Engineering on the Degree Certificate.

3. What is the difference between a Deemed University and an Autonomy College?

A Deemed University is fully autonomous to the extent of awarding its own Degree. A Deemed University is usually a Non-Affiliating version of a University and has similar responsibilities like any University. An Autonomous College enjoys Academic Autonomy alone. The University to which an autonomous college is affiliated will have checks on the performance of the autonomous college.

4. How will the Foreign Universities or other stake – holders know that we are an Autonomous College?

Autonomous status, once declared, shall be accepted by all the stake holders. Foreign Universities and Indian Industries will know our status through our college website.

5. What is the change of Status for Students and Teachers if we become Autonomous?

An autonomous college carries a prestigious image. Autonomy is actually earned out of continued past efforts on academic performances, capability of self-governance and the kind of quality education we offer.

6. Who will check whether the academic standard is maintained / improved after Autonomy? How will it be checked?

There is a built in mechanism in the autonomous working for this purpose. An Internal Committee called Academic Programme Evaluation Committee is a Non – Statutory body, which will keep a watch on the academics and keep its reports and recommendations every year. In addition to Academic Council, the highest academic body also supervises the academic matters. At the end of three years, there is an external inspection by the University for this purpose. The standards of our question papers, the regularity of academic calendar, attendance of students, speed and transparency of result declaration and such other parameters are involved in this process.

7. Will the students of VCE as an Autonomous College qualify for University Medals and Prizes for academic excellence?

No. VCE has instituted its own awards, medals, etc. for the academic performance of the students. However for all other events like sports, cultural and co-curricular organized by the University the students shall qualify.

8. Can VCE have its own Convocation?

No, since the University awards the Degree the Convocation will be that of the University.

9. Can VCE give a provisional degree certificate?

Since the examinations are conducted by VCE and the results are also declared by VCE, the college sends a list of successful candidates with their final percentage of marks to the University. Therefore with the prior permission of the University the college will be entitled to give the provisional certificate.

10. Will Academic Autonomy make a positive impact on the Placements or Employability?

Certainly. The number of students qualifying for placement interviews is expected to improve, due to rigorous and repetitive classroom teaching and continuous assessment, besides the autonomous status is more responsive to the needs of the industry. As a result, there will be a lot of scope for

industry oriented skill development built-in into the system. The graduates from an autonomous college will therefore represent better employability.

11. What is the proportion of Internal and External Assessment as an Autonomous College?

Presently, it is 25 % for internal assessment and 75 % for external assessment. As the autonomy matures the internal assessment component shall be increased at the cost of external assessment.

12. Will there be any Revaluation or Re-Examination System?

No. There will not be any Revaluation system or Re-examination. But, there is a personal verification of the answer scripts.

13. How fast Syllabi can be and should be changed?

Autonomy allows us the freedom to change the syllabi as often as we need.

14. Will the Degree be awarded on the basis of only final year performance?

No. The percentage of marks will reflect the average performance of all the semesters put together.

15. Who takes Decisions on Academic matters?

The Academic Council of College is the top academic body and is responsible for all the academic decisions. Many decisions are also taken at the lower level like the BOS which are like Boards of Studies of the University.

16. What is the role of Examination committee?

The Exam Committee is responsible for the smooth conduct of inter and external examinations. All matters involving the conduct of examinations, spot valuations, tabulations, preparation of Memorandum of Marks etc fall within the duties of the Examination Committee.

17. Is there any mechanism for Grievance Redressal?

Yes, the college has grievance redressal committee, headed by a senior faculty member of the college.

18. How many attempts are permitted for obtaining a Degree?

All such matters are defined in Rules & Regulations.

19. Who declares the result?

The result declaration process is also defined. After tabulation work the entire result is reviewed by the Moderation Committee. Any unusual deviations or gross level discrepancies are deliberated and removed. The entire result is discussed in the College Academic Council for its approval. The result is then declared on the college notice boards as well put on the web site of the college. It is eventually sent to the University.

20. What is our relationship with the Jawaharlal Nehru Technological University, Hyderabad?

We remain an affiliated college of the Jawaharlal Nehru Technological University, Hyderabad. The University has the right to nominate its members on the academic bodies of the college.

21. Shall we require University approval if we want to start any New Courses?

Yes, It is expected that approvals or such other matters from an autonomous college will receive priority.

22. Shall we get autonomy for PG and Doctoral Programmes also?

Yes, presently our PG programmes are also enjoying autonomous status.

23. How many exams will be there as an autonomous college?

This is defined in the Rules & Regulations.